

Docket No. A1WI2376US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Douglas W. Babcock, Robert A. Duris,
Bruce Hecht

Serial No. 10/722,970

Filed: November 25, 2003

Title: AUTOMATIC TEST EQUIPMENT PIN CHANNEL WITH
T-COIL COMPENSATION

Commissioner for Patents
Mail Stop Amendment
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF ROBERT A. DURIS

I, Robert A. Duris, declare:

1. I am a co-inventor of the invention which is the subject of the above-identified patent application.

2. At all times mentioned herein I was, and am presently, a Senior Staff Engineer for Analog Devices, Inc. (ADI), the assignee of the invention and patent application.

3. Attached as Exhibit 1 is a copy of a slide presentation I gave on April 13, 2000 at the annual ADI General Technical Conference, entitled "Integrated Bridged T-Coils for ATE Pin Electronics". This is an internal conference within ADI intended to brief employees on new developments within the company that have not yet become public. My presentation was confidential to ADI, and the slides were marked "ADI Proprietary." The slides documented

Best Available Copy



my concept of the invention, and disclosed the invention as claimed in the application.

4. Attached as Exhibit 2 is an annotated copy of selected figures from Exhibit 1, marked up as follows to show the correspondence between the figure elements and the elements of the application claims:

Page 2: This figure illustrates a bridged T-Coil circuit that can be used for the "passive matching network" of the claims, as described in the specification at page 9, line 30-page 10, line 7.

Page 4: This figure illustrates the problem which the invention addresses, with a circuit that includes the "ATC bidirectional drive channel", "device under test (DUT)", "input/output line for connection to a DUT", "driver circuit", "receiver circuit" and "associated capacitance" of the receiver circuit recited in claim 1 of the application, but not the passive matching network of claim 1.

Page 6: This figure is similar to the page 4 figure up to the DUT, but shows the addition of the "first passive matching network to at least partially compensate for receiver circuit capacitance" connected to the input/output line of claim 1. The "passive matching network" is shown implemented as a "T-coil circuit" as in claim 2. Instead of the single driver circuit on page 4, it shows the driver circuit implemented as the combination of current-mode and voltage-mode driver circuits as in claim 5.

Page 7: This figure is similar to the page 6 figure, but instead of the simple "passive matching network" on page 6 it shows two passive matching networks as in claim 5, with the second passive matching network "connected in series with the first passive matching network to at least partially compensate for the current-mode driver capacitance" as in claim 5. Both passive matching networks are shown implemented as respective T-coils, as in claim 6.

Page 10: This figure illustrates the T-coil circuit including "inductors that are implemented in a separate layer" of an integrated circuit (IC) that is spaced by at least a dielectric layer from a "common layer" on which the driver and receiver circuits are implemented, as in claim 3.

Page 40: This page displays a photograph of a chip layout to implement the invention as claimed in claims 1, 5 and 6, discussed above.

5. On May 25, 2000 a circuit design to implement the invention was released to the ADI fabrication facility. Attached as Exhibit 3 is a copy of IC chip layouts dated May 23, 2000, marked-up to show the claimed elements of the invention, including T-coil circuits that were internal to the chip and implemented in its metal-3 layer.

6. On August 22, 2000 a first wafer lot was received from the ADI fabrication facility, and on September 15, 2000 a second wafer lot was received. The second lot had

the same functional circuitry as the first lot, but the location of connection vias was changed to allow for the addition of post-passivation T-coils external to the chip. The internal T-coils implemented in the metal-3 layer were of aluminum approximately three microns thick, whereas post-passivation T-coils were of copper or gold up to ten microns thick. It was believed that internal T-coils would be functional, but that post-passivation T-coils would perform better. Exhibit 4 is a copy of a test trace that was obtained from the wafer received August 22, 2000, performed the same day, showing that both the current-mode driver (A) and the voltage-mode driver (AB) were functional.

7. The development of test software to test the second T-coil wafer lot began on September 15, 2000 when the wafer lot was received, and was completed on September 20, 2000. On the latter date the circuits on the second wafer lot were tested; a printout of the test results is appended as Exhibit 5. Of the 95 circuits tested, 24 had metal-3 T-coils. The test results are summarized on the first page of Exhibit 5. The last line of this page indicates a yield of 17/24 for the metal-3 T-coils circuits, meaning that 17 of the 24 circuits tested worked properly. Only DC testing was performed at this time, which did not show whether the T-coil circuits successfully compensated for the receiver circuit capacitance. The testing was performed by Daniel Sheehan, an API employee.

8. On September 20, 2000 the second lot wafers were sent to Advanced MicroSensors, Inc., an independent

company, for the addition of post-passivation T-coils. The completed wafers, including post-passivation T-coils, were returned to ADI on October 12, 2000. A copy of the Advanced MicroSensors cover letter transmitting the completed wafers is attached as Exhibit 6. Copies of photographs taken by Advance MicroSensors of the post-passivation T-coils are attached as Exhibit 7.

9. Beginning upon the receipt of the post-passivation T-coil wafers on October 12, 2000, ADI developed a characterization setup in its characterization laboratory to test and characterize the drive channel circuits to which Advanced MicroSystems had added post-passivation T-coils. A circuit with the post-passivation T-coils was tested on October 17, 2000, and a copy of a trace of the results is attached as Exhibit 8, plotting ρ as a function of time. ρ is a measure of impedance matching; the results show a negative peak of about -120mp. A similar circuit but without post-passivation T-coils was tested on October 18, 2000, and a copy of a trace of the results is attached as Exhibit 9. This trace shows a negative peak of about -260mp, which indicated that the addition of the post-passivation T-coils was successful in substantially compensating the receiver circuit capacitance. Both tests were made by Robert Bombara, an ADI employee.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge

that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: May 30, 2006


Robert A. Duris

(V)NR/RBR/ABand/D, of Robert A. Duris ALW123Y6051

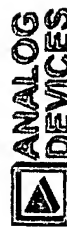
Integrated Bridged T-Coils for ATE Pin Electronics

Presented by

Bob Duris

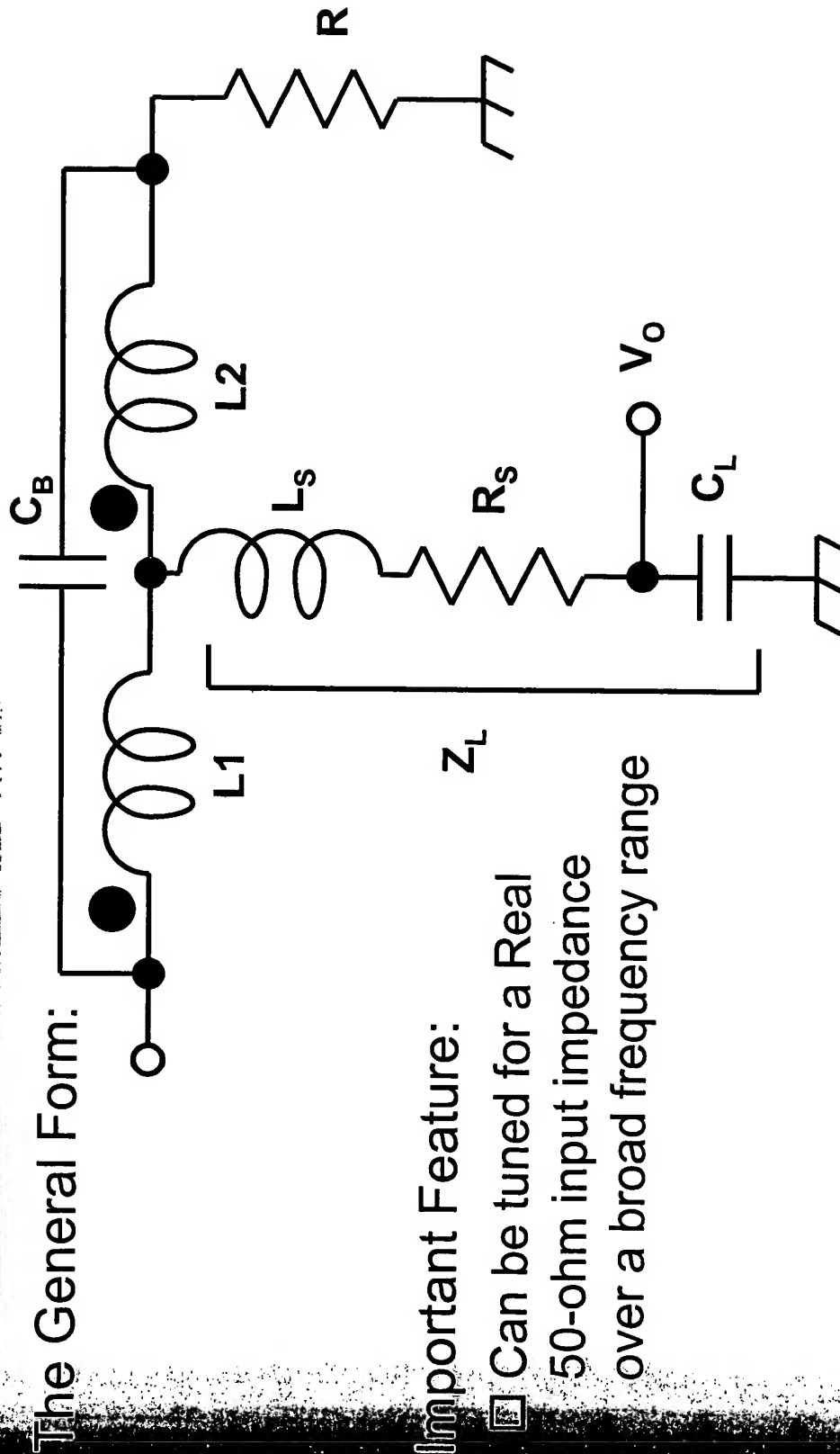
ATE Products Group

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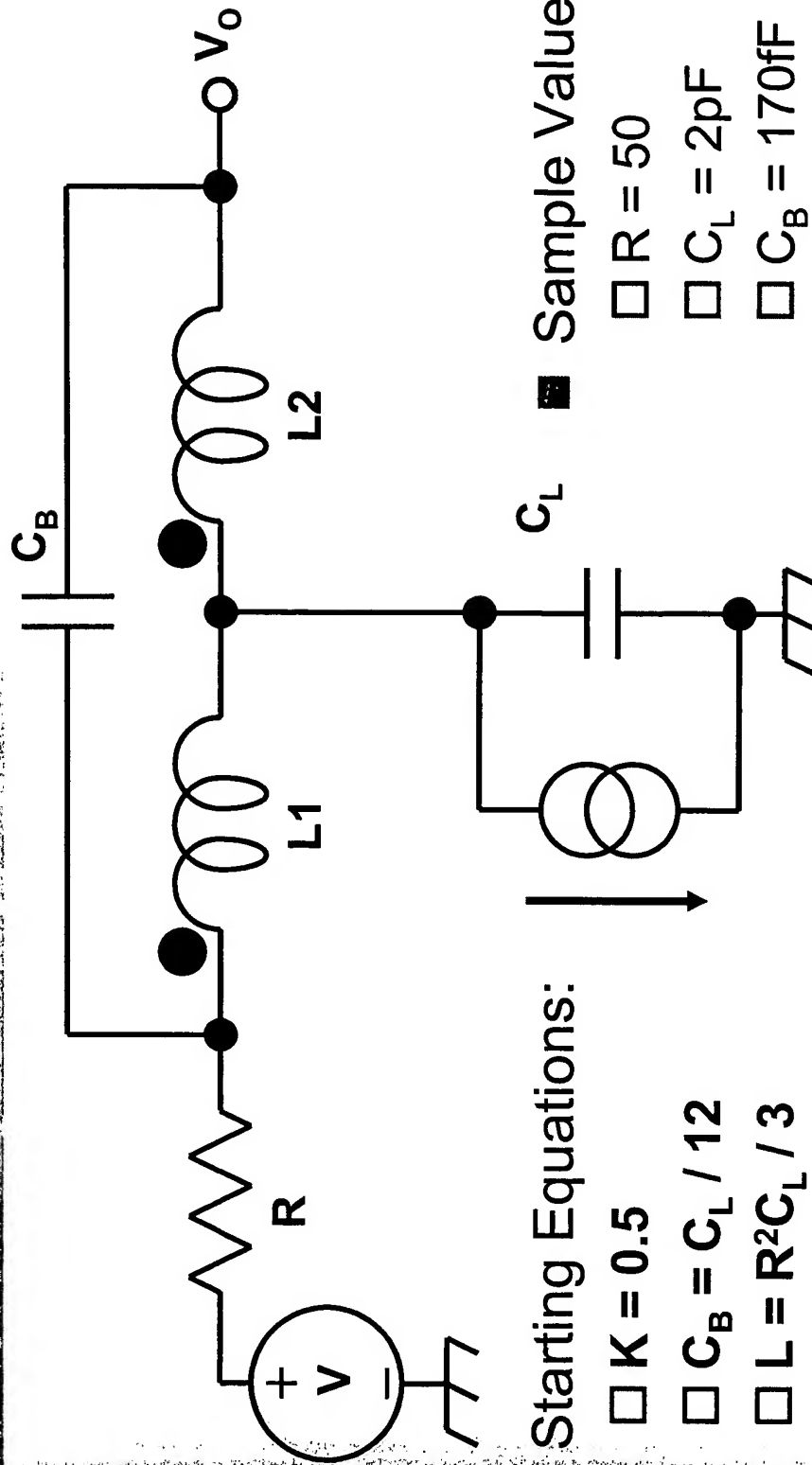


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What is a Bridged T-Coil?



Simplified Balanced Bridged T-Coil



Starting Equations:

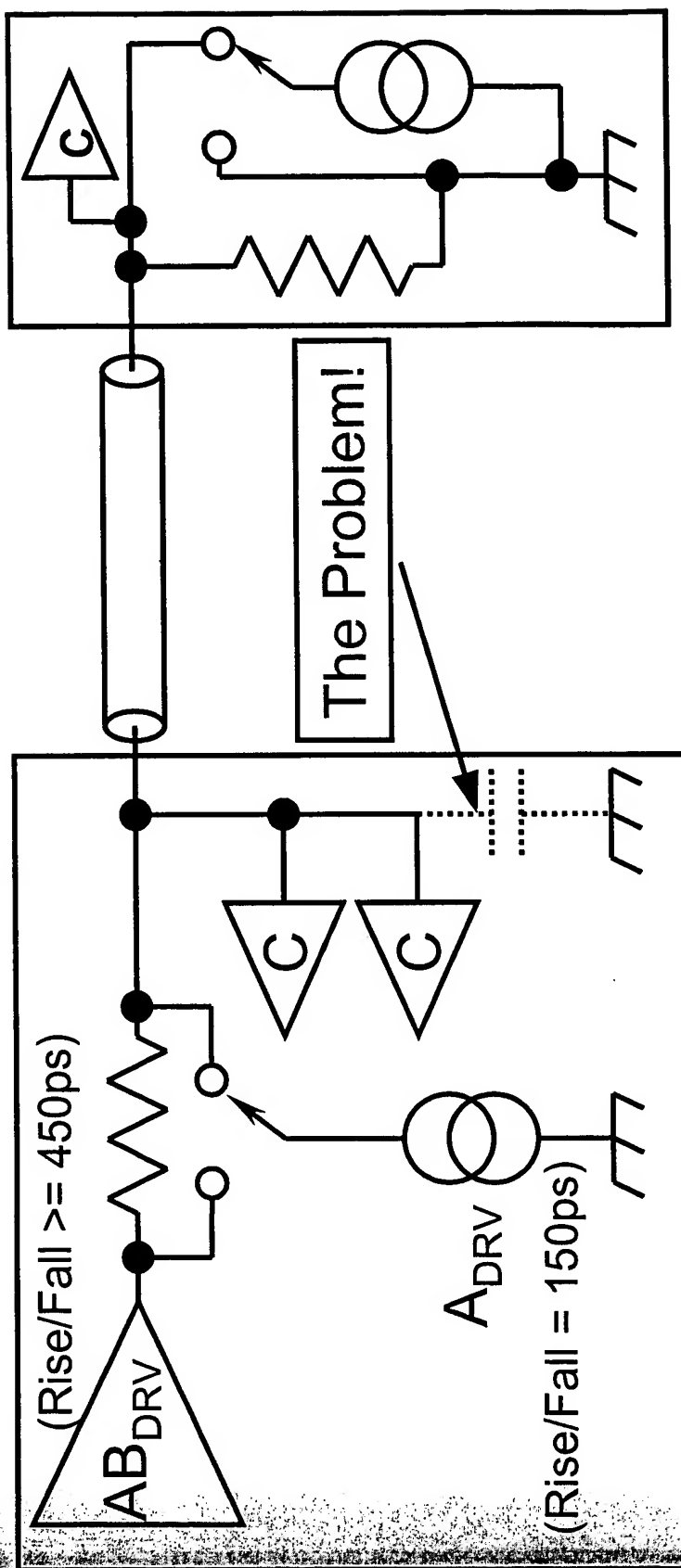
- $\square K = 0.5$
- $\square C_B = C_L / 12$
- $\square L = R^2 C_L / 3$

Sample Values:

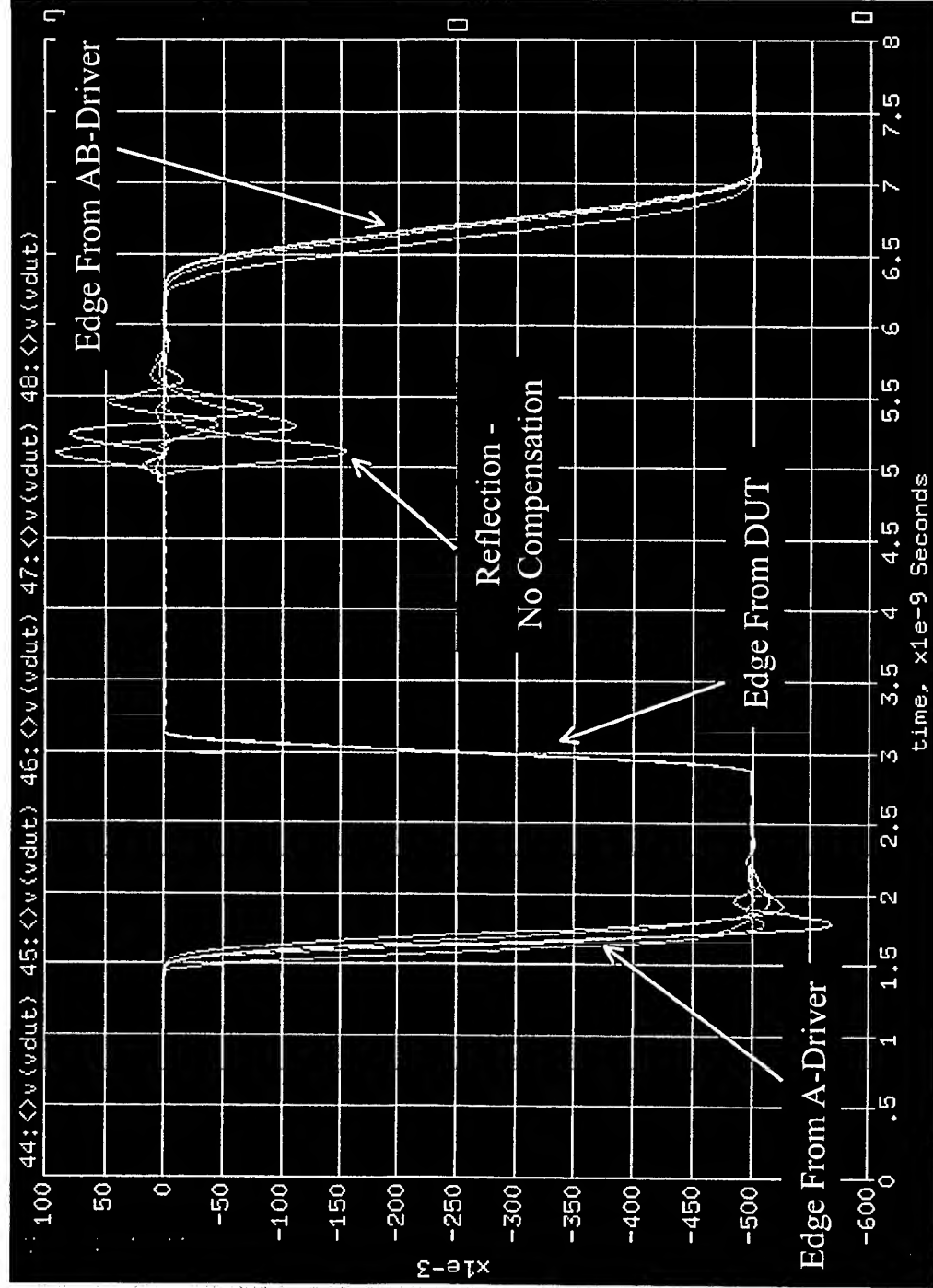
- $\square R = 50$
- $\square C_L = 2\text{pF}$
- $\square C_B = 170\text{fF}$
- $\square L = 1.6\text{nH}$

What problem are we trying to solve?

■ ATE Tester Pin Channel



An Example Waveform (DUT End)

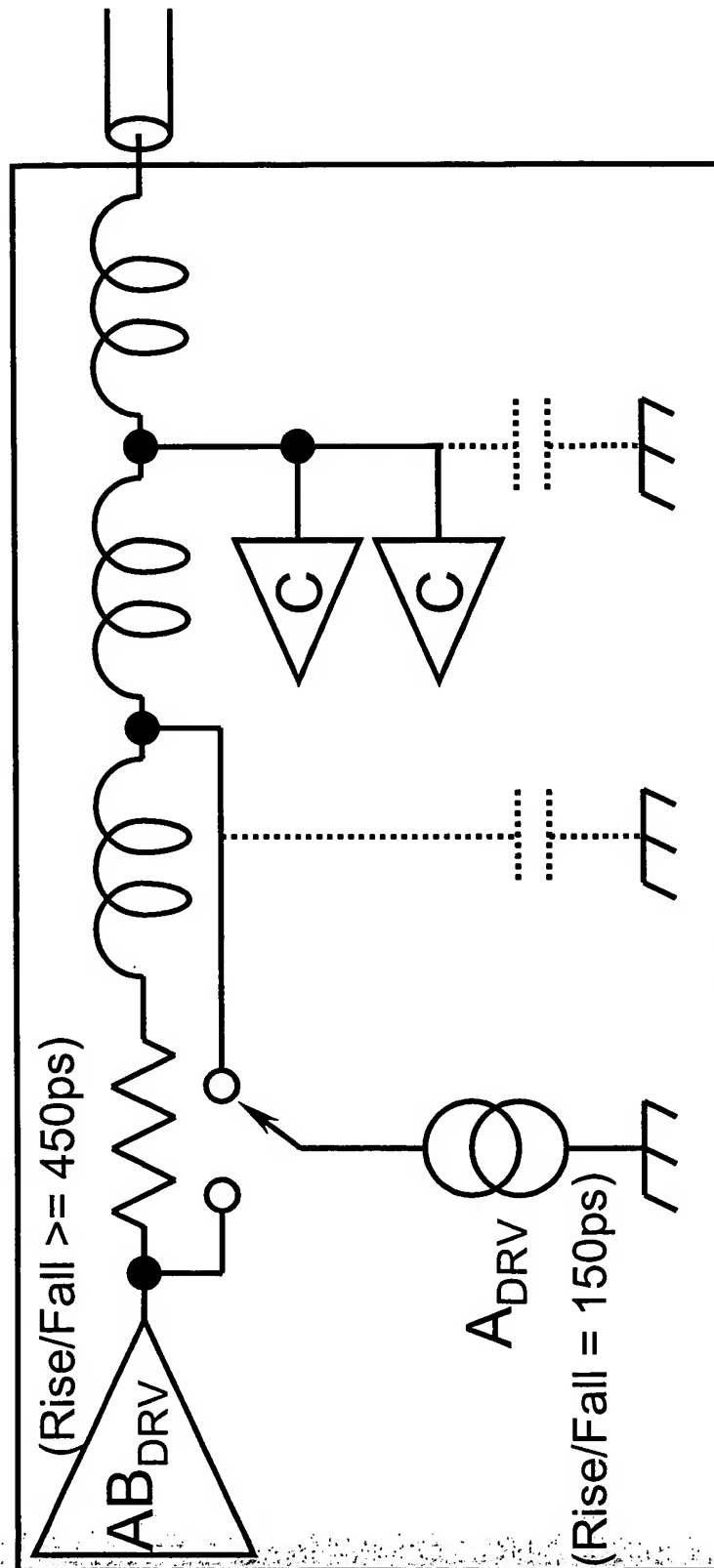


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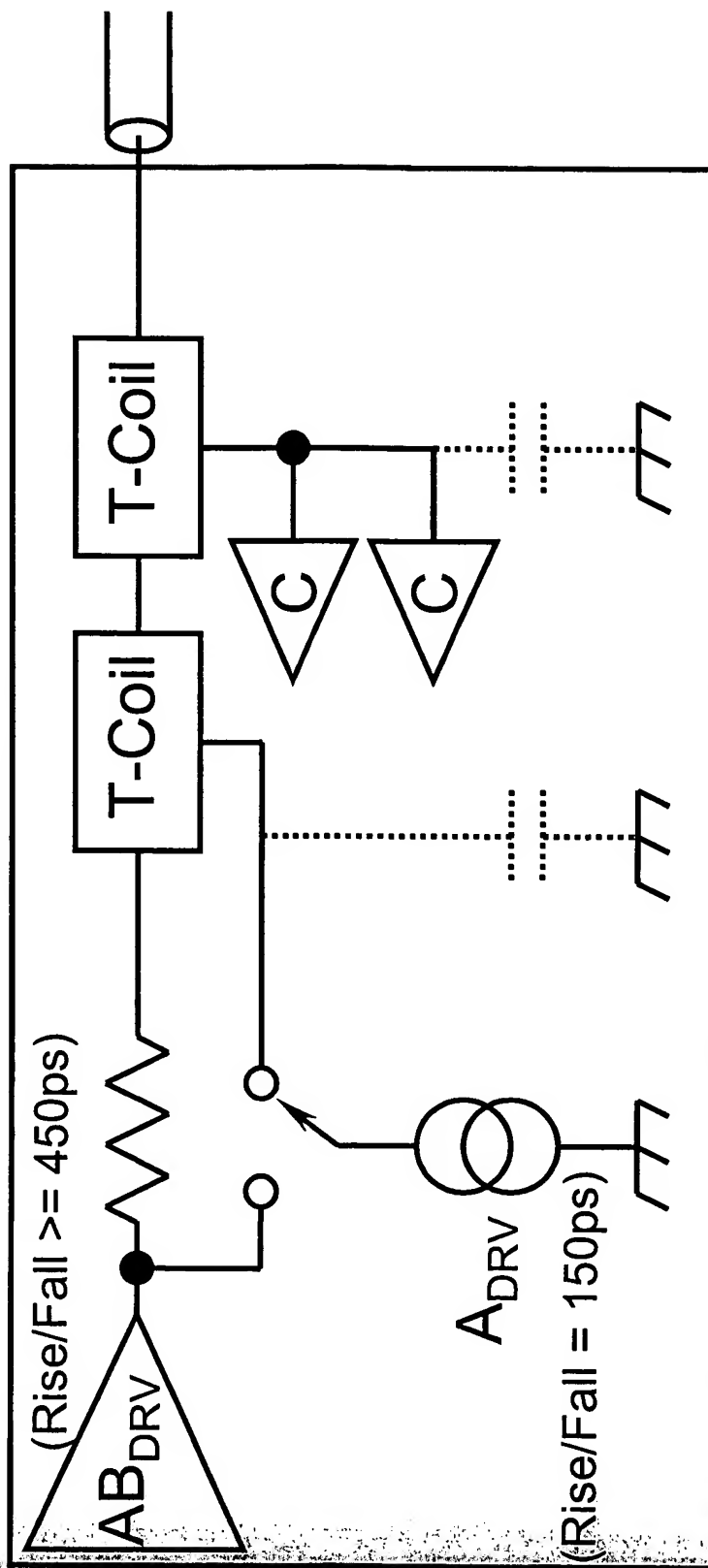
How Do We Compensate?

■ Inductors



How Do We Compensate?

■ T-Coils



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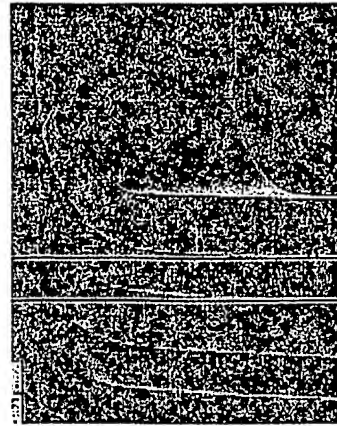
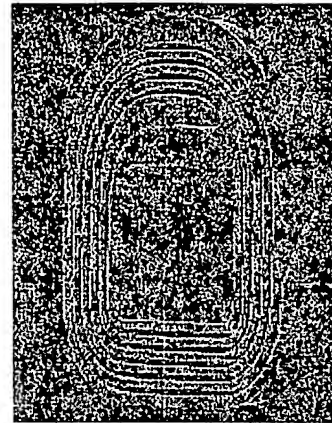
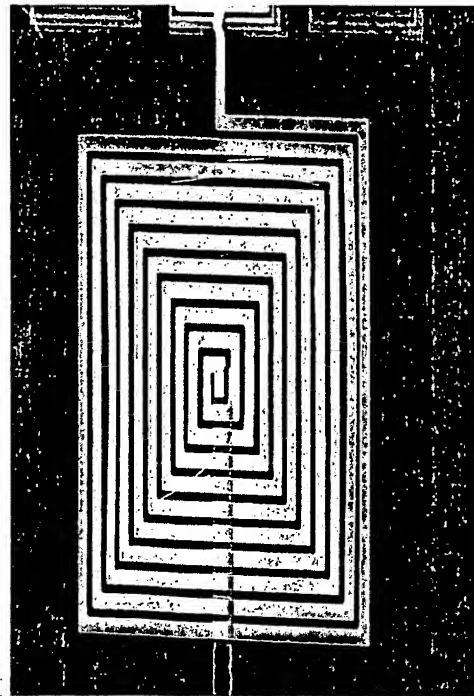
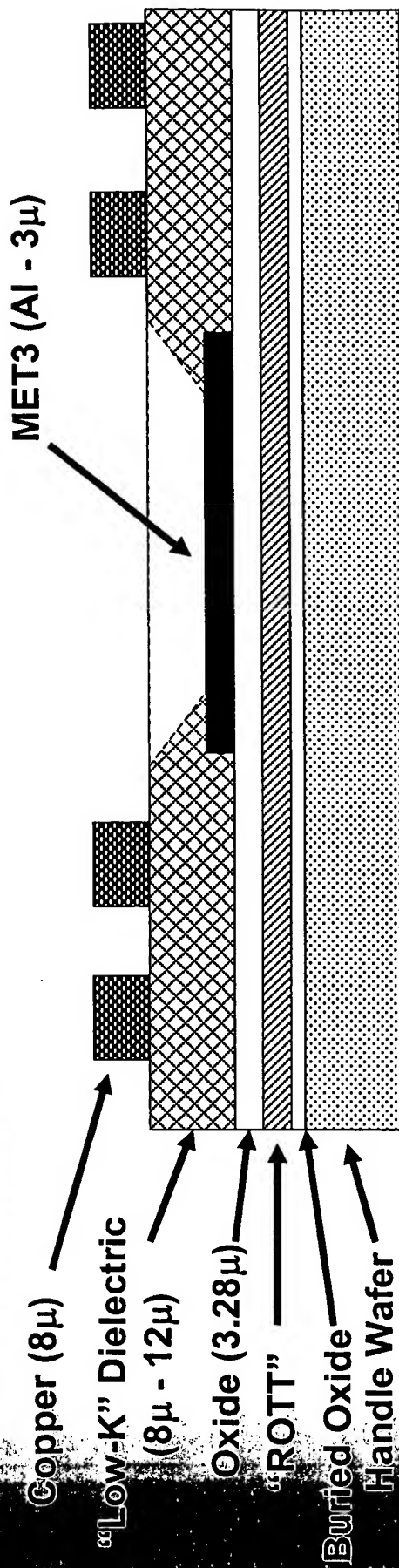
Key Inductor Performance Issues

- Low Resistance
- High “Q”
- Low Capacitance
- Small Size
- ADI Semiconductor Process Compatible

What Processes Are Available?

- MET3 Inductors On XF2 - 3 μ M Thick Aluminum
- CU Inductors, 8 μ M Thick Post-Processed on 12 μ M of Low-K Dielectric (K=2.7) (MEMSCAP)
- CU Inductors, 8 μ M Thick Post-Processed on 8 μ M of Low-K Dielectric (K=2.7) (Advanced MicroSensors)
- Other: Chip-On-Chip, Bond Wires, etc.

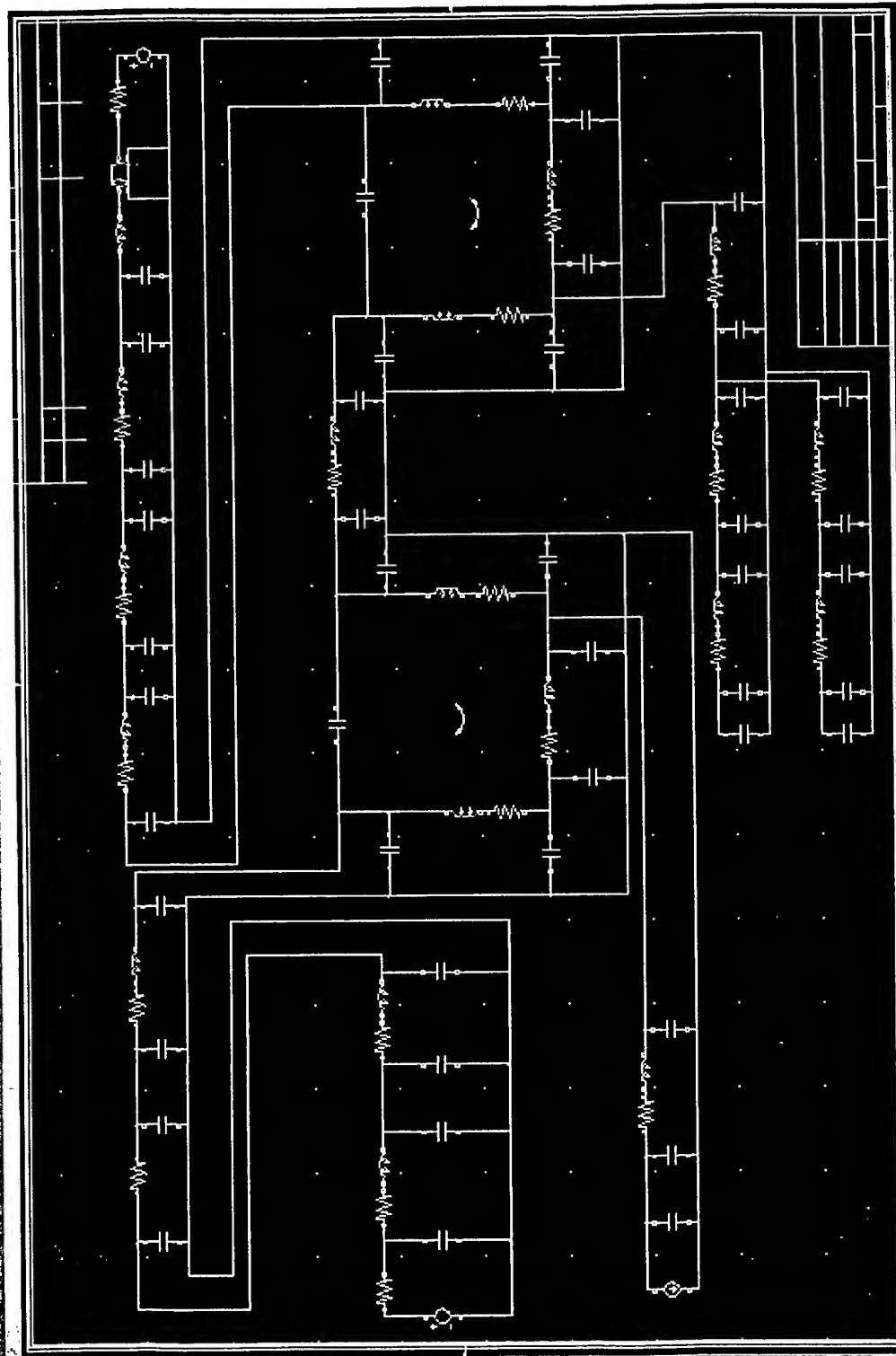
What Do The Post-Processed Structures Look Like?



How Well Do T-Coils Work?

- Process Comparison: None, MET3, AMS, MEMSCAP
- Comparison to None, 1, 2 and 3-Inductor Compensation
- Single Vs. Dual T-Coils
- Sensitivity to:
 - ☐ Inductance Value
 - ☐ Comparator Capacitance
 - ☐ Class-A Driver Capacitance
 - ☐ Metal Parasitic Capacitance
 - ☐ Inductor Coupling Coefficient
 - ☐ Bridge Capacitor Value
 - ☐ Trace and Coil Series Resistance

Simulation Schematic

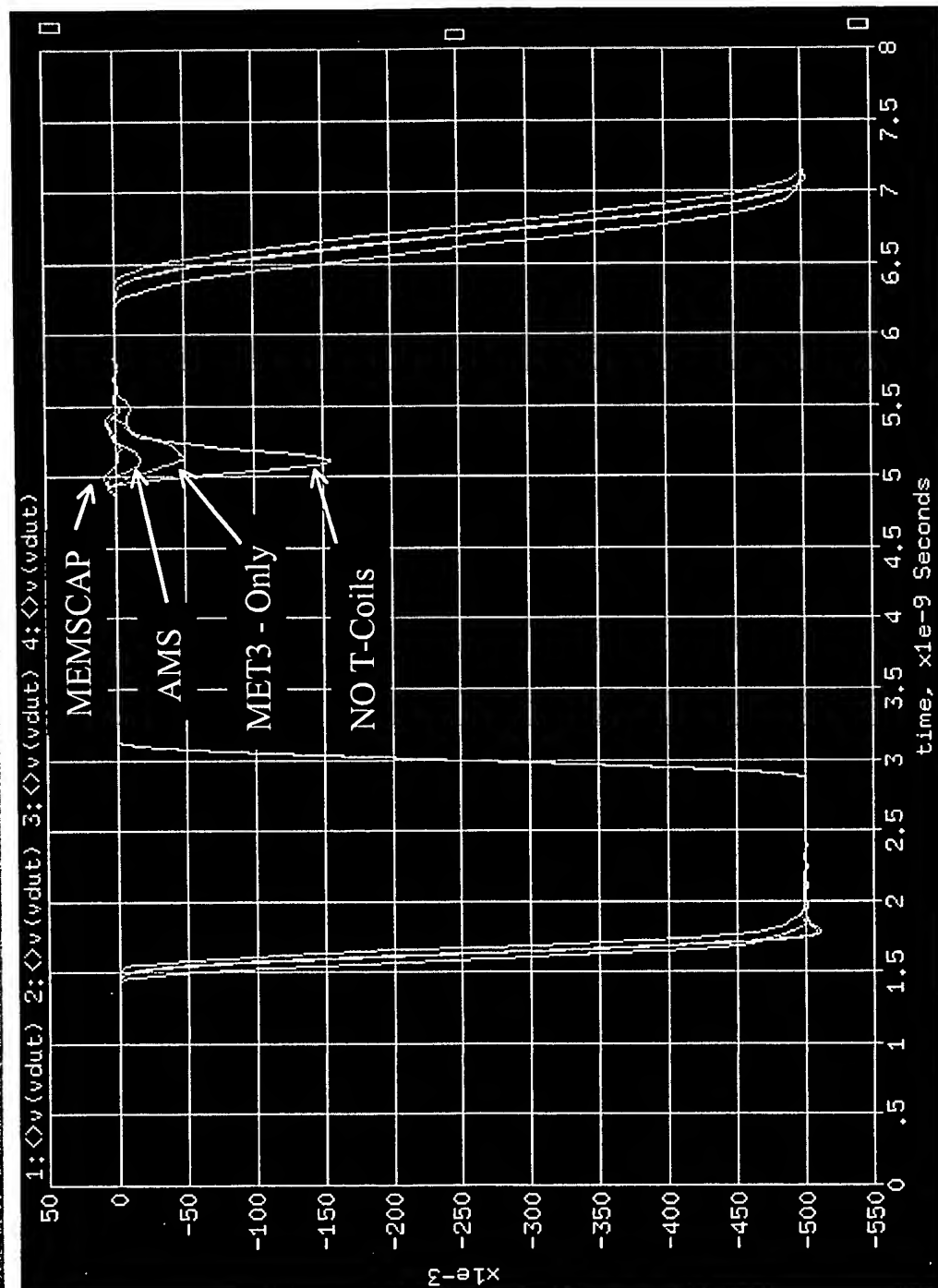


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T-Coils Compared by Process

Composite Overview Waveform at DUT



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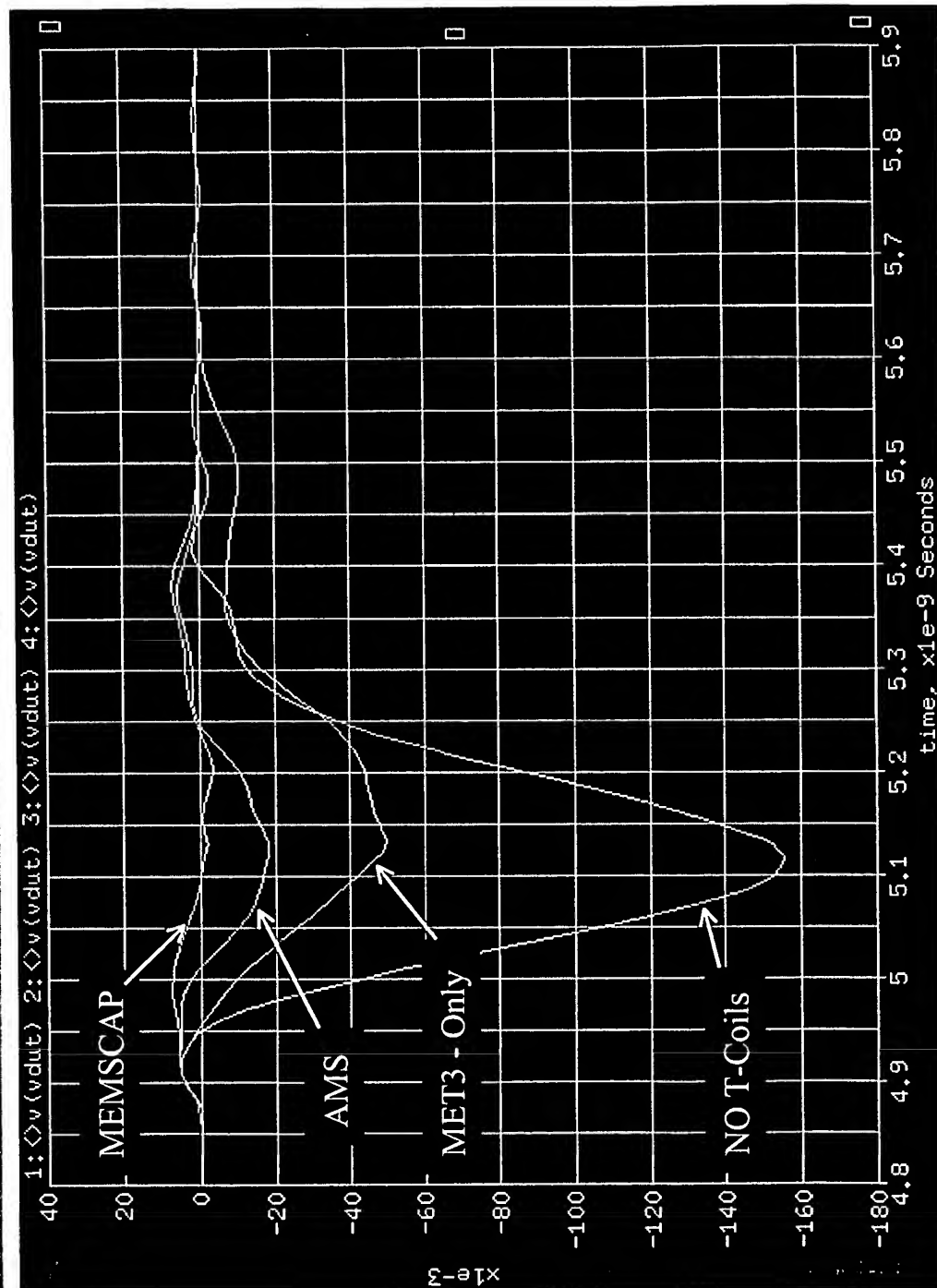
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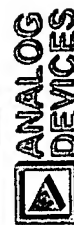
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T-Coils Compared by Process

Composite Overview Waveform at DUT - Reflection



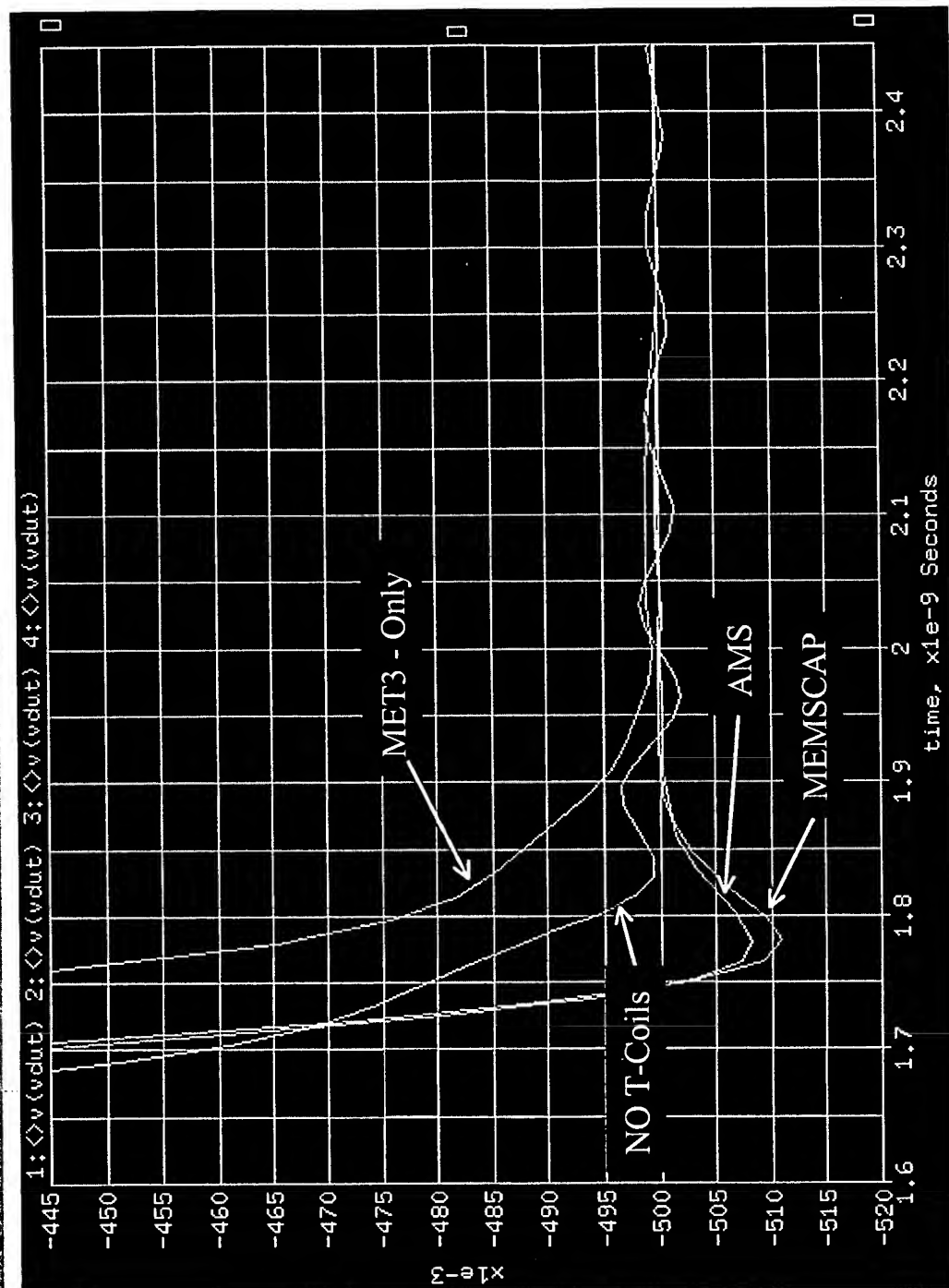
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T-Coils Compared by Process

Composite Overview Waveform at DUT - Incident Edge



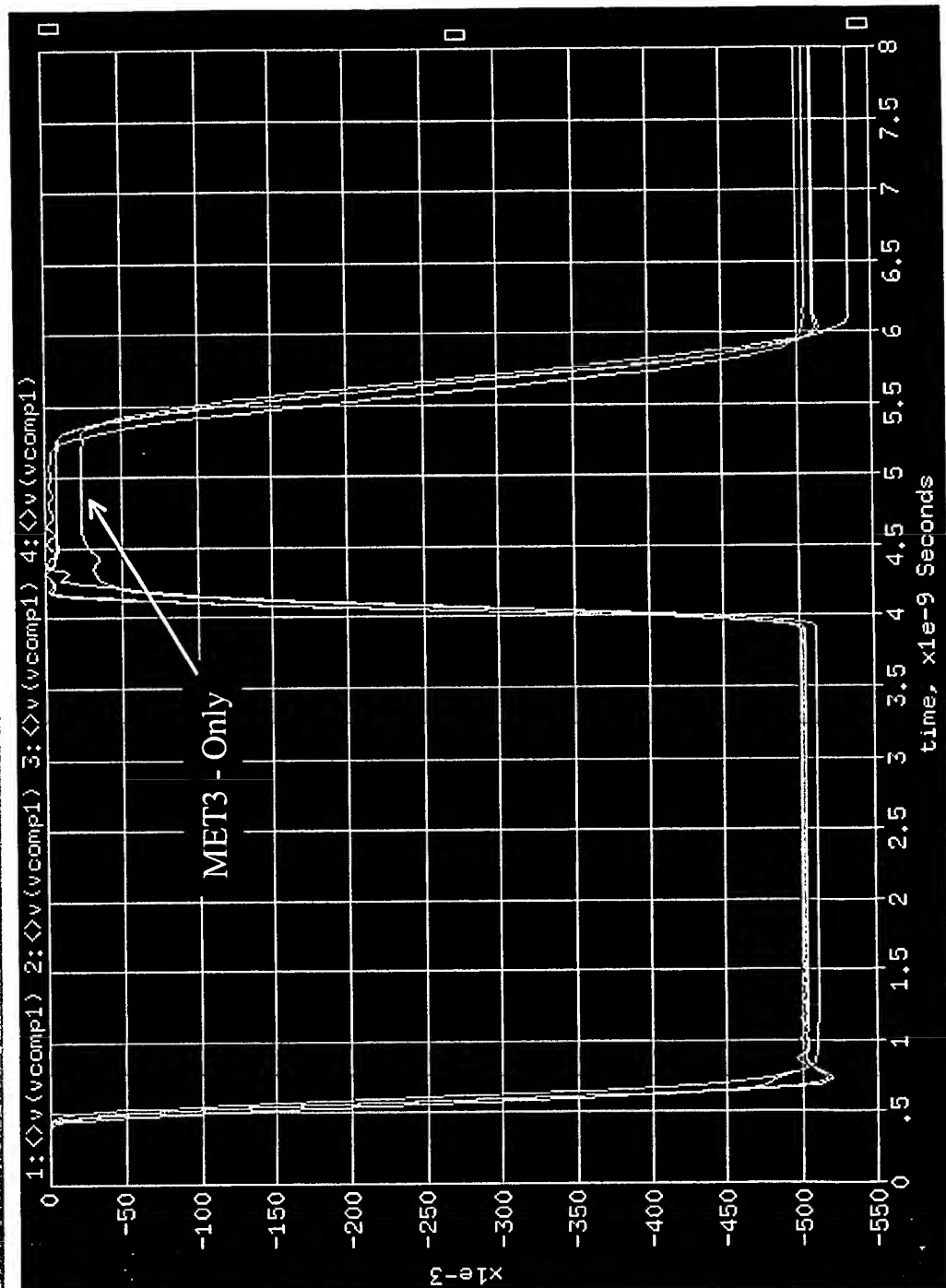
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T-Coils Compared by Process

Composite Overview Waveform at Comparator

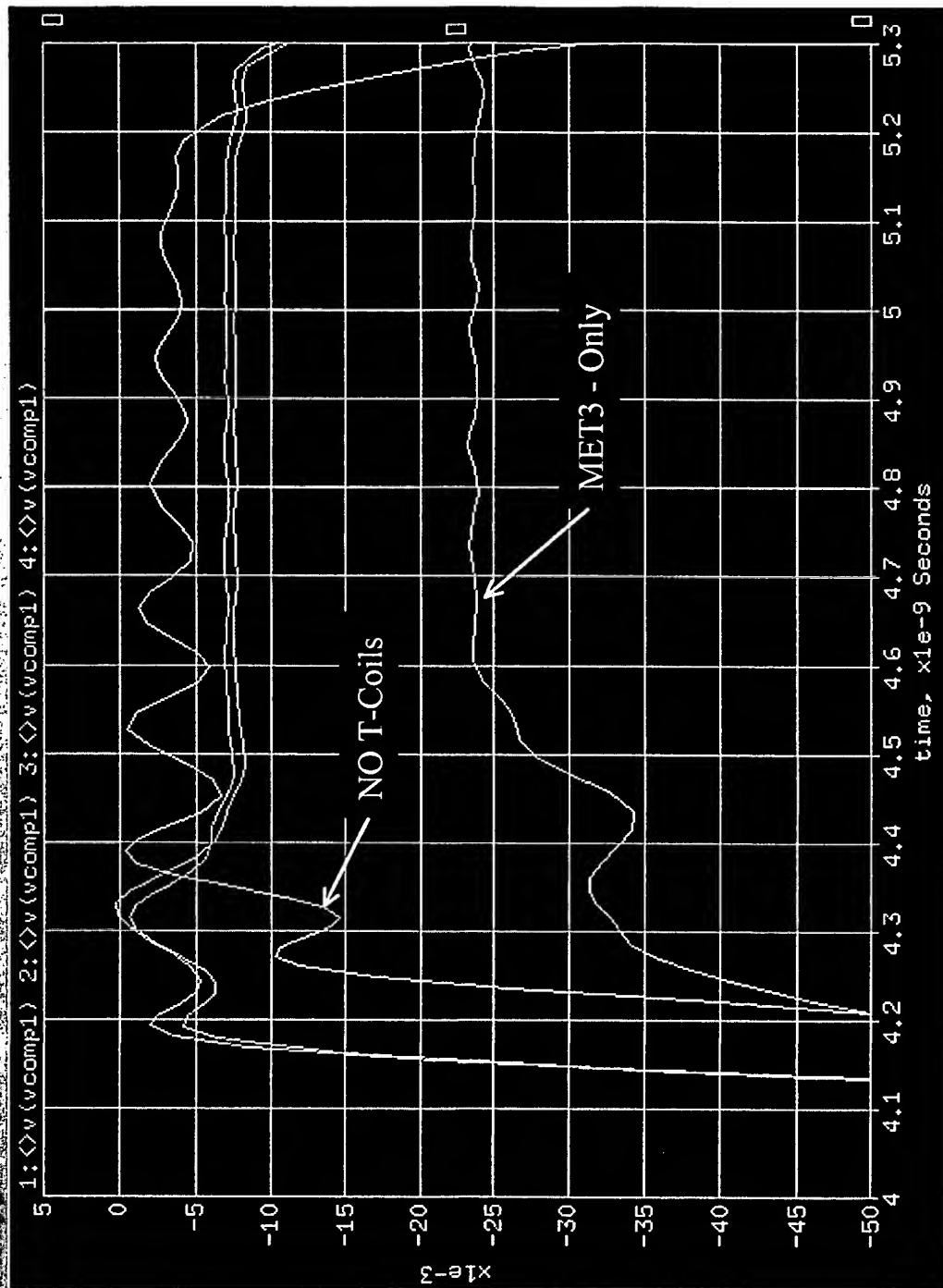


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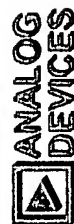
T-Coils Compared by Process

■ Composite Overview Waveform at Comparator Enlarged



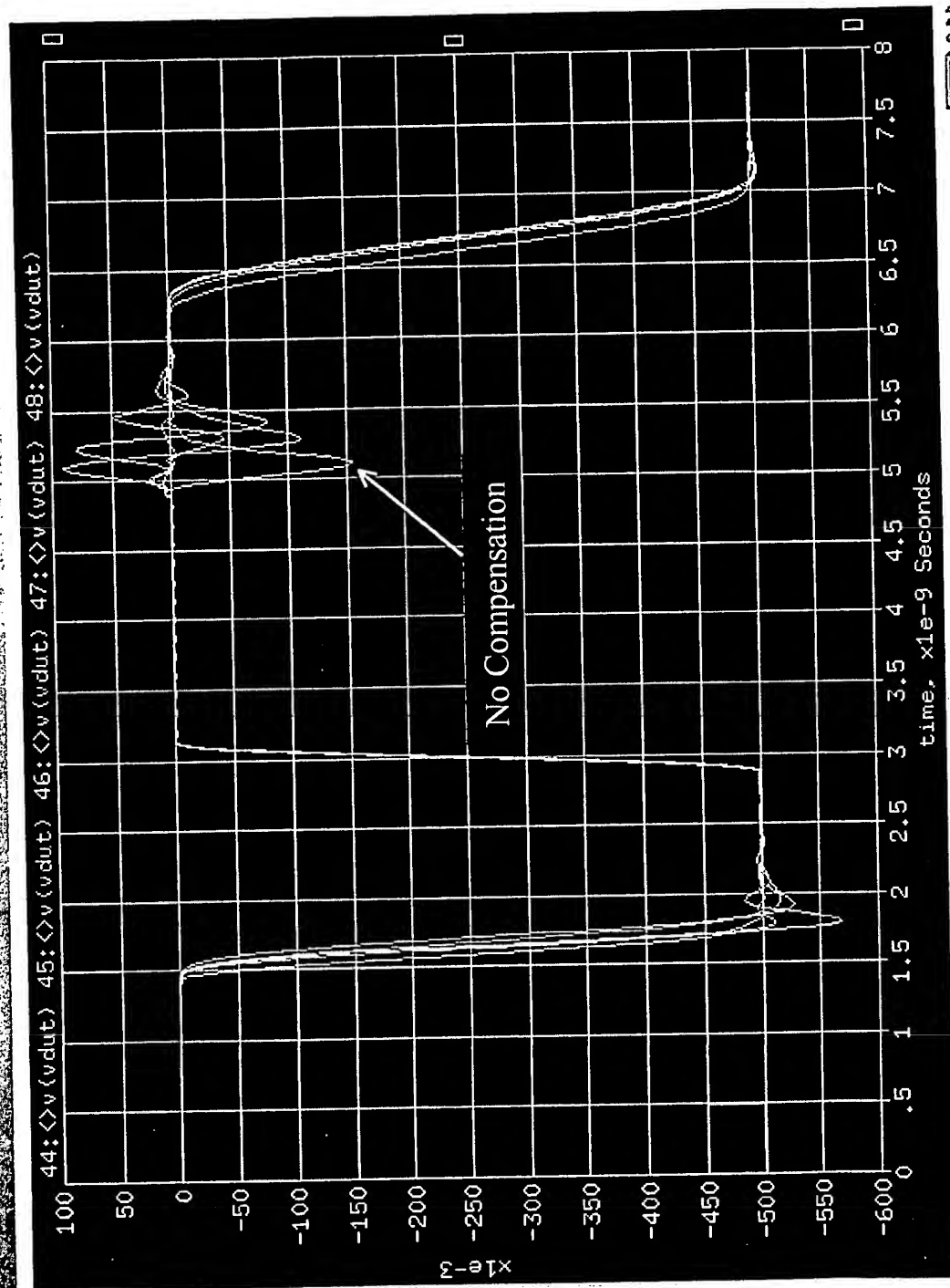
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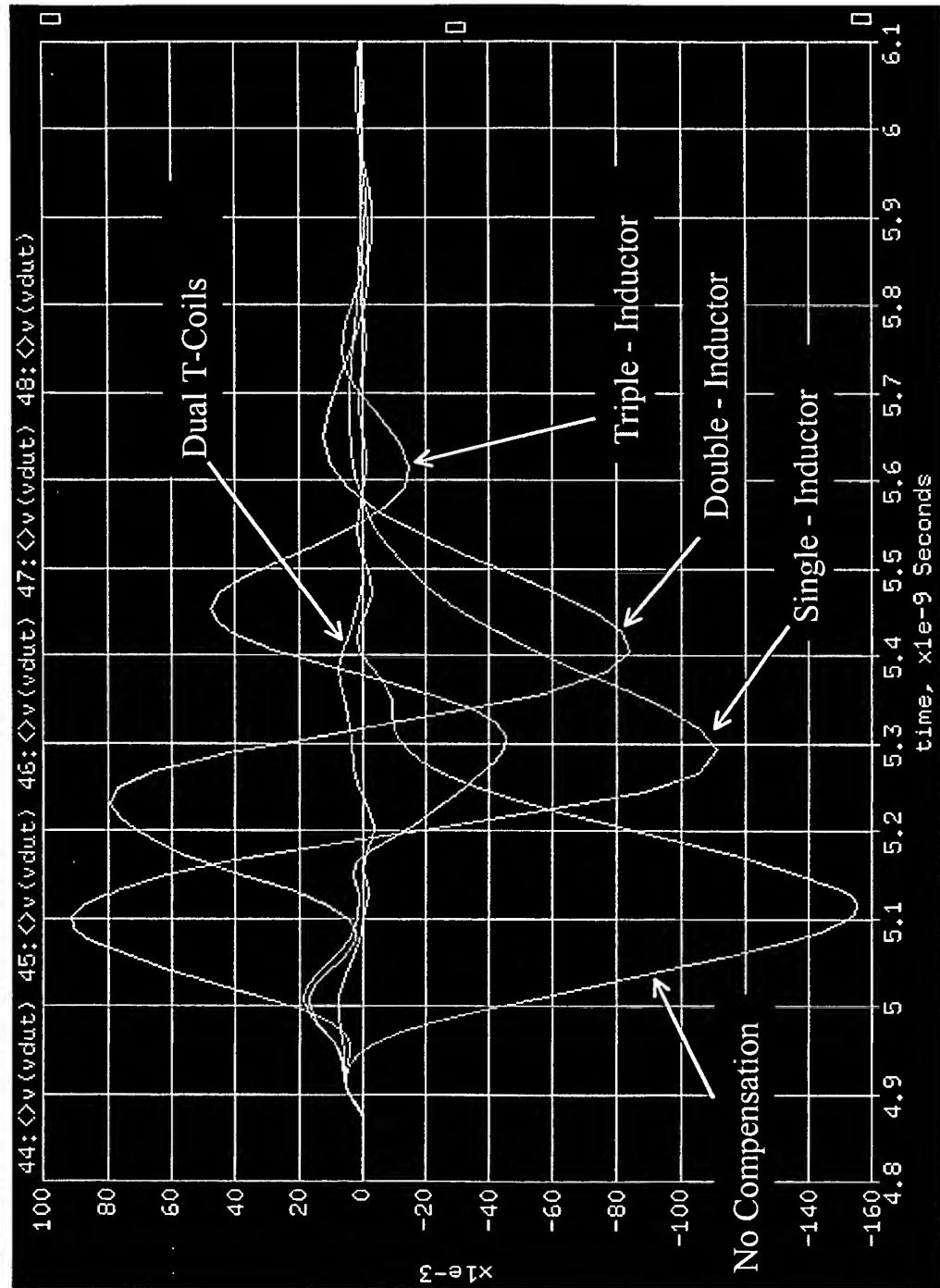
T-Coils Compared To 0, 1, 2, 3 Inductors

Composite Overview Waveform at DUT



T-Coils Compared To 0, 1, 2, 3 Inductors

Composite Overview Waveform at DUT - Reflection



ADI Proprietary

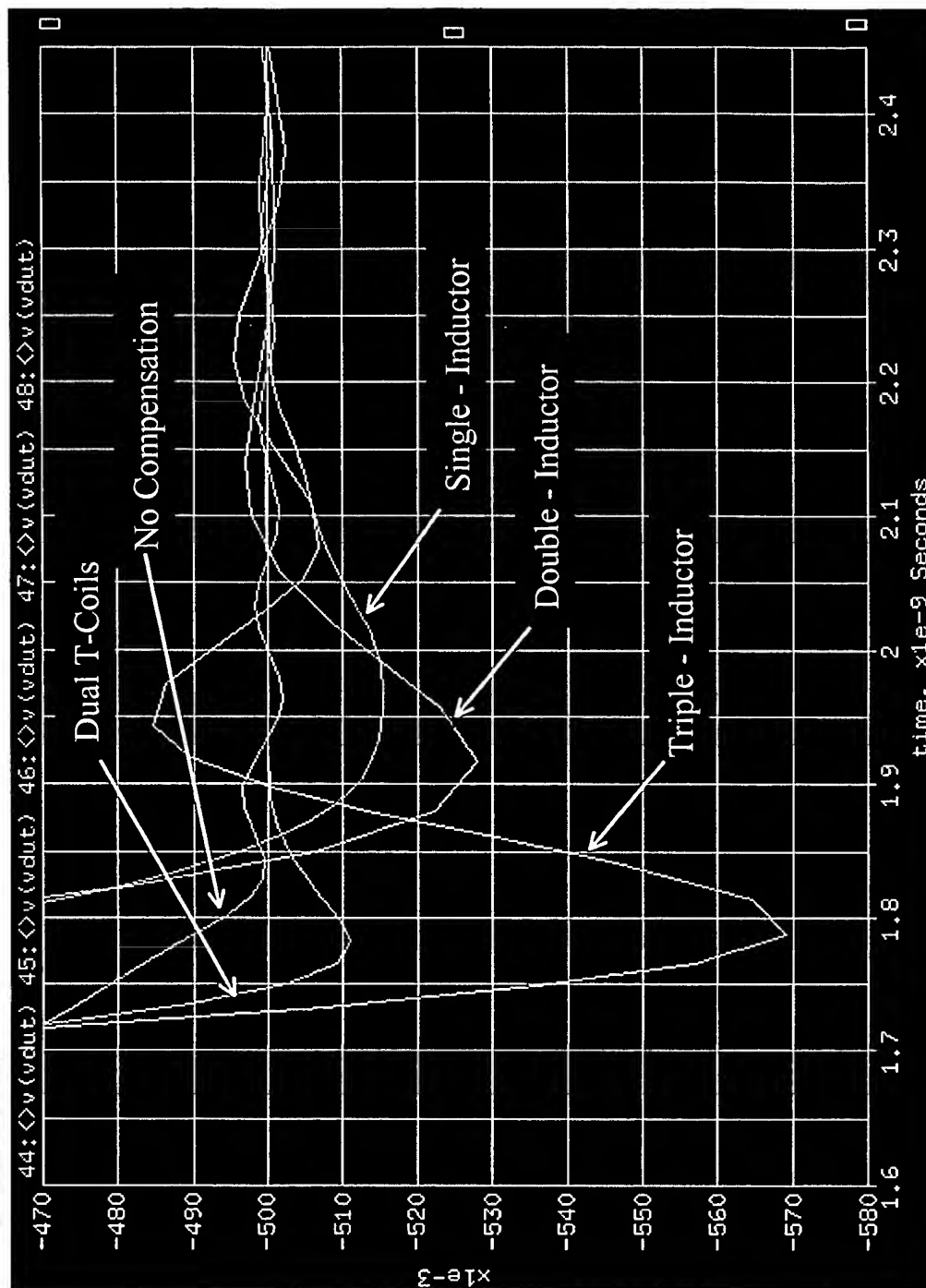
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T-Coils Compared To 0, 1, 2, 3 Inductors

■ Composite Overview Waveform at DUT - Incident Edge



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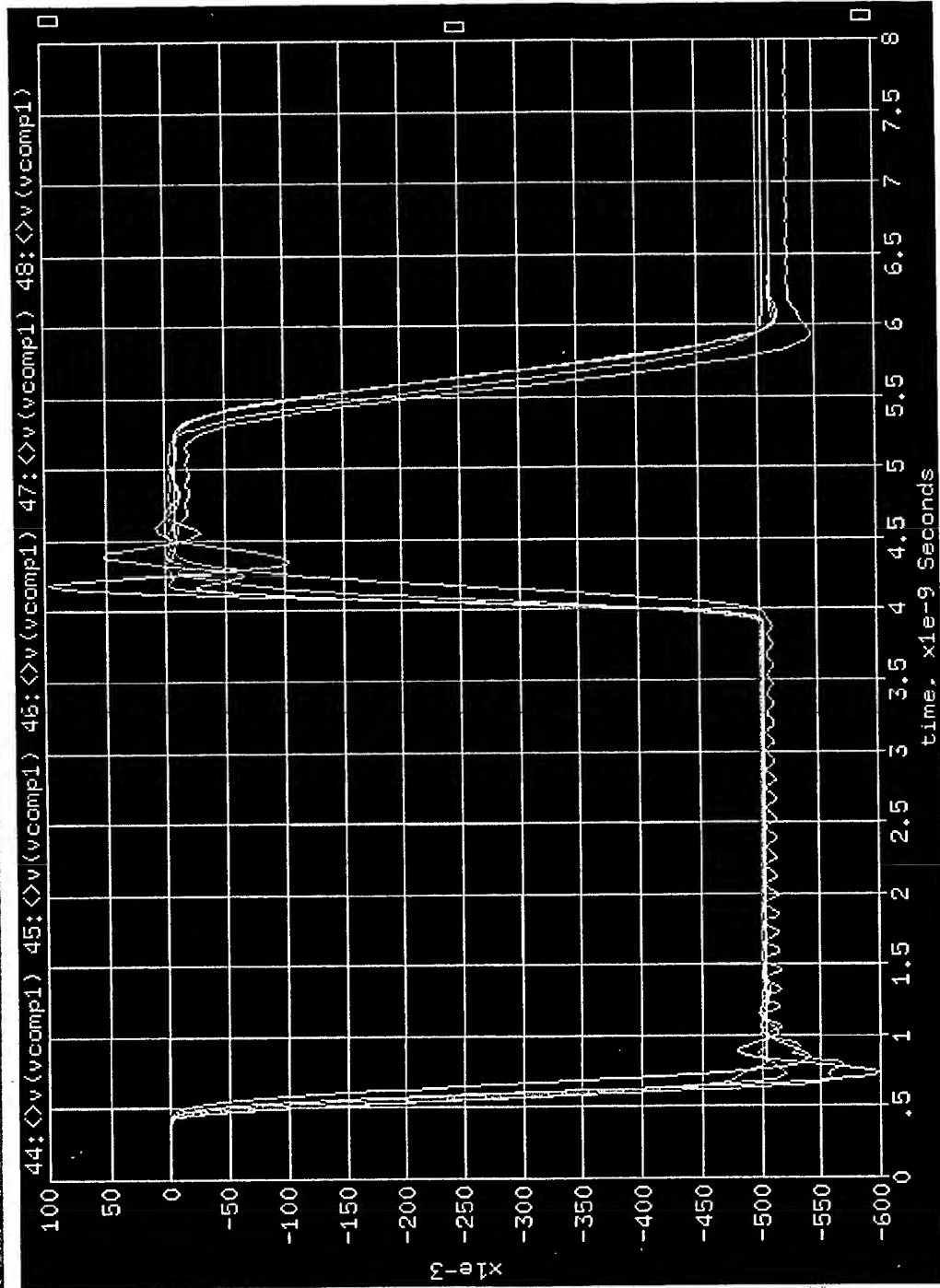
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T-Coils Compared To 0, 1, 2, 3 Inductors

Composite Overview Waveform at Comparator

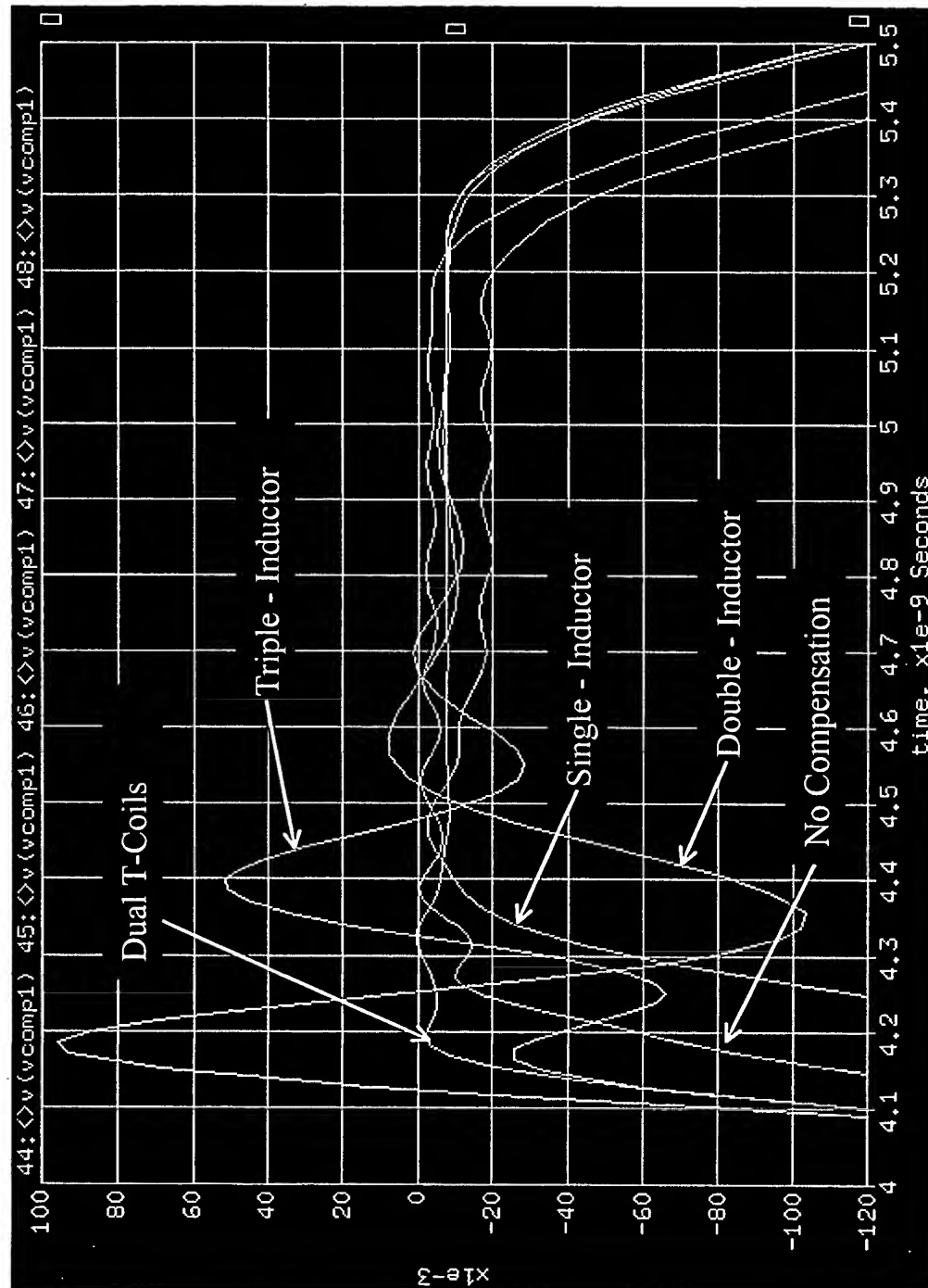


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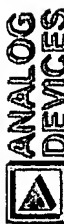
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ANALOG
DEVICES

T-Coils Compared To 0, 1, 2, 3 Inductors

Composite Overview Waveform at Comparator Enlarged



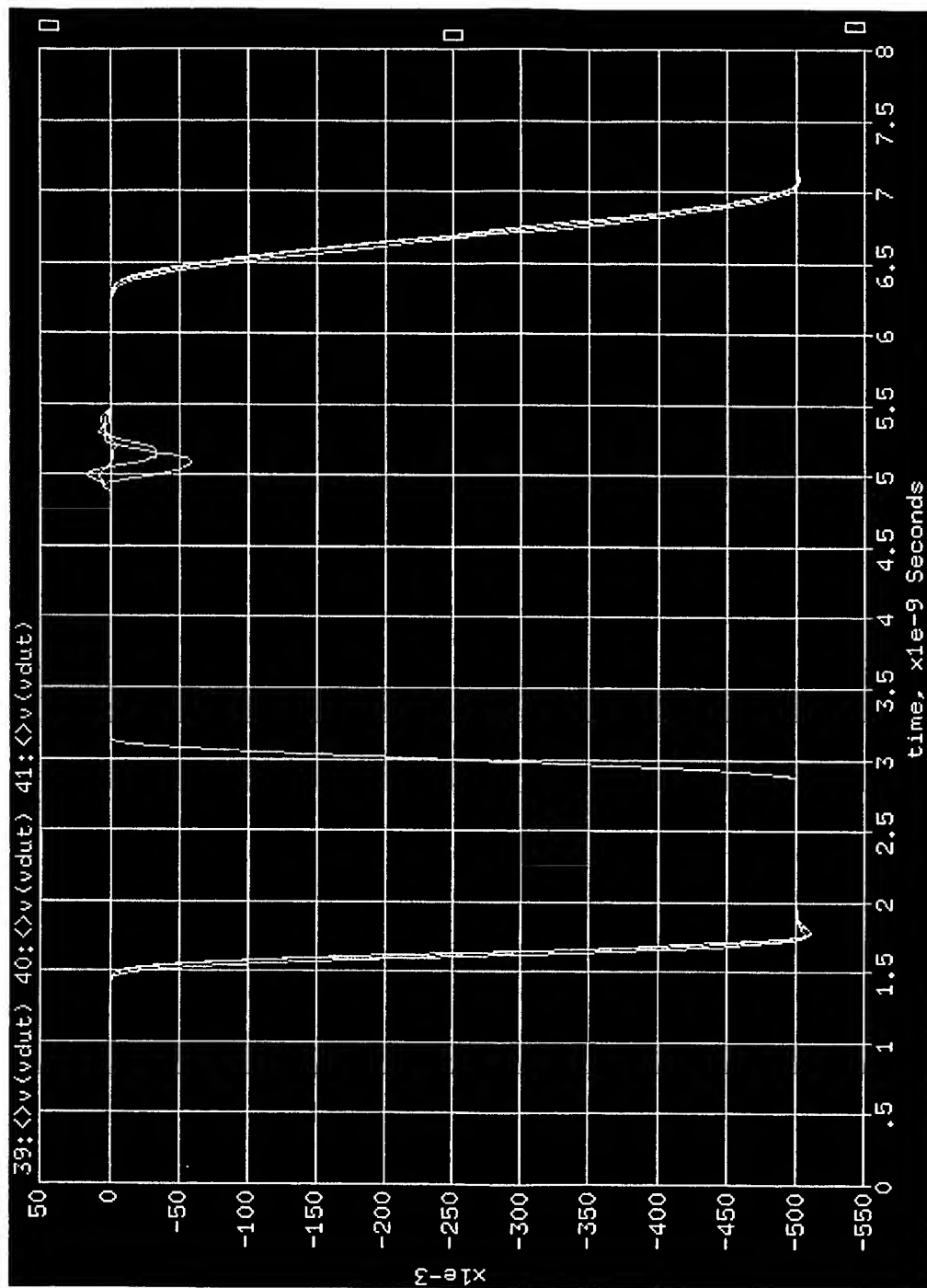
ADI Proprietary
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One Vs. Two T-Coils Compared

■ Composite Overview Waveform at DUT



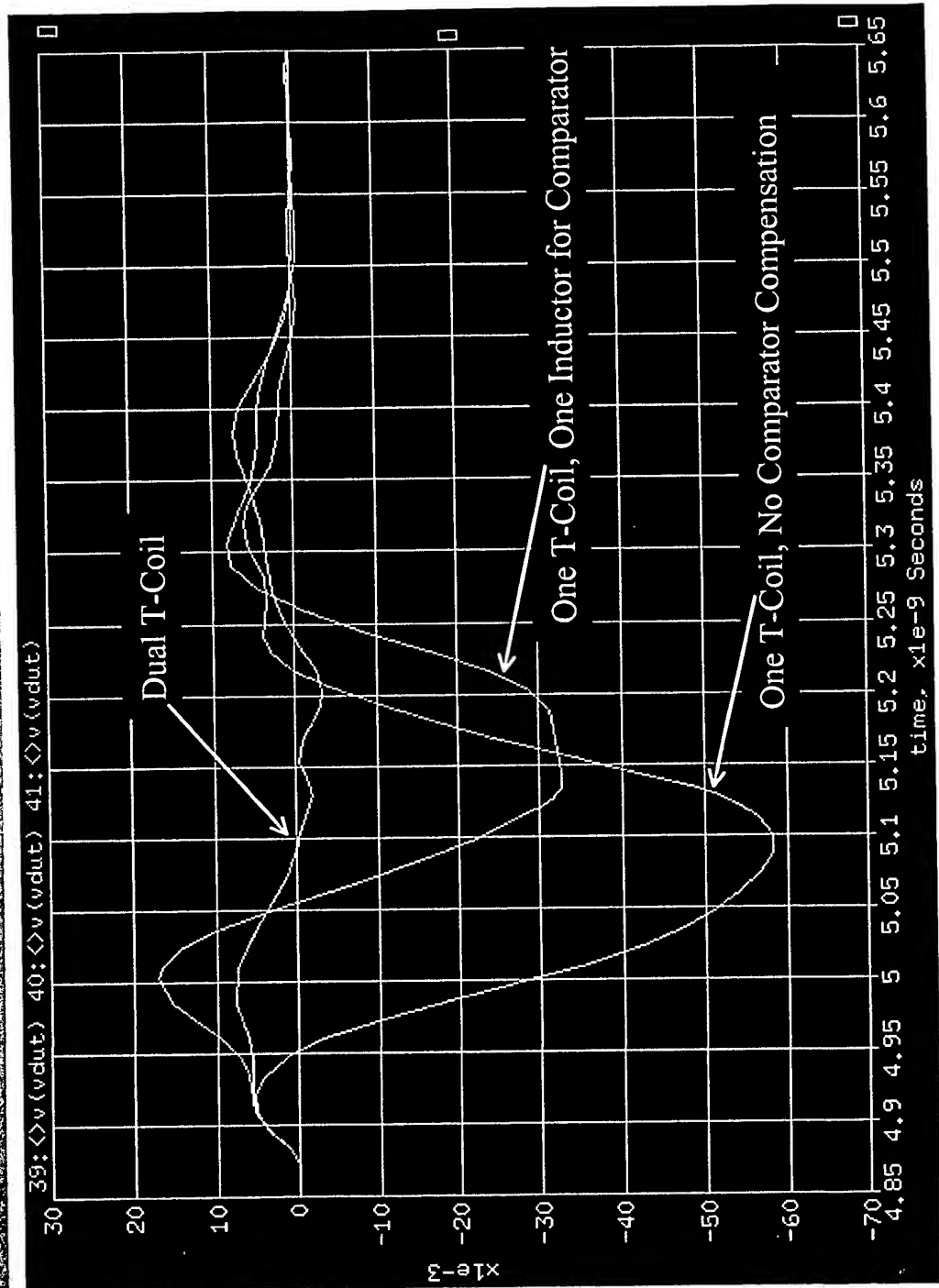
ADI Proprietary
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One Vs. Two T-Coils Compared

Composite Overview Waveform at DUT - Reflection



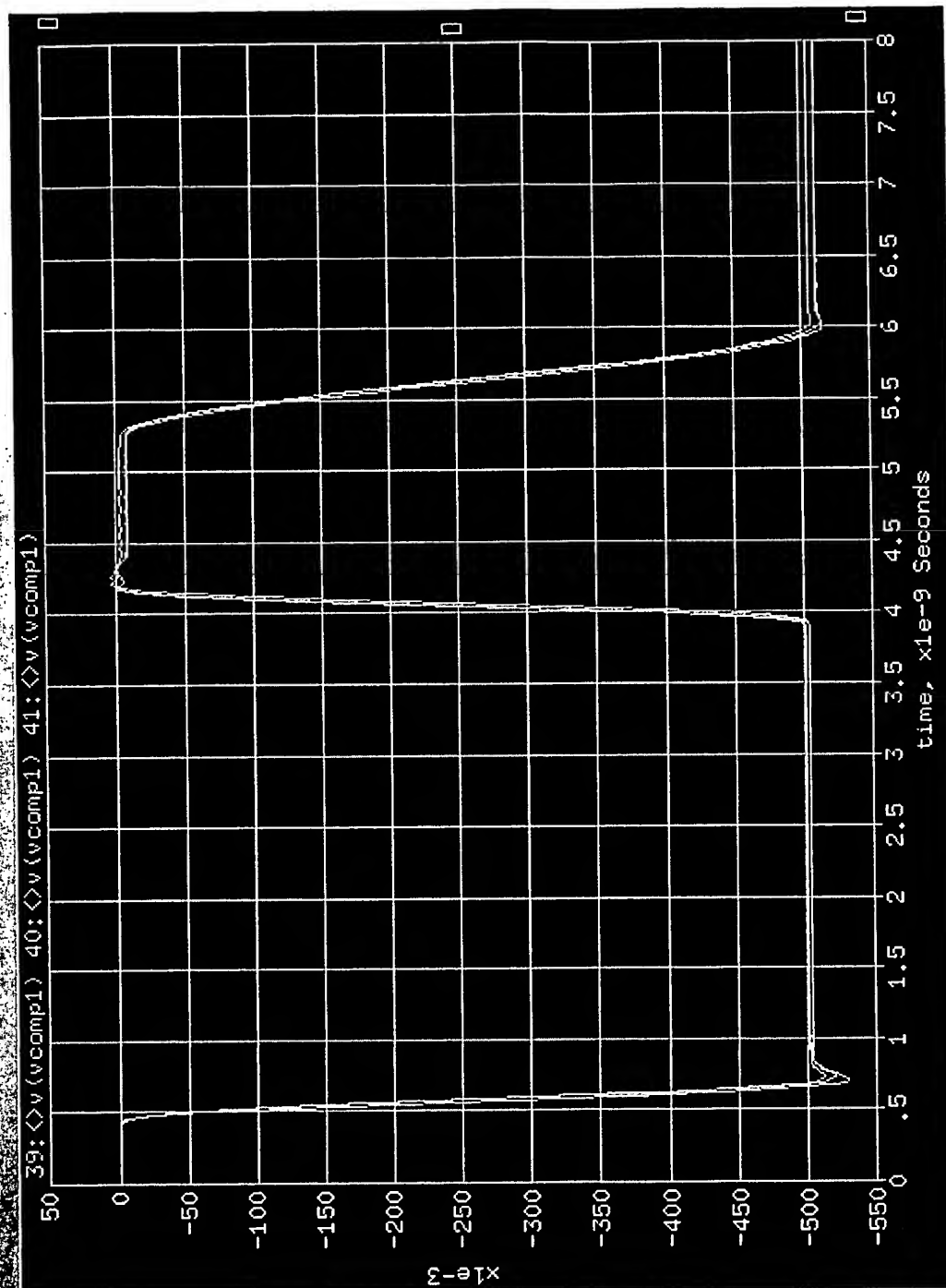
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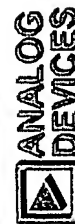
One Vs. Two T-Coils Compared

Composite Overview Waveform at Comparator



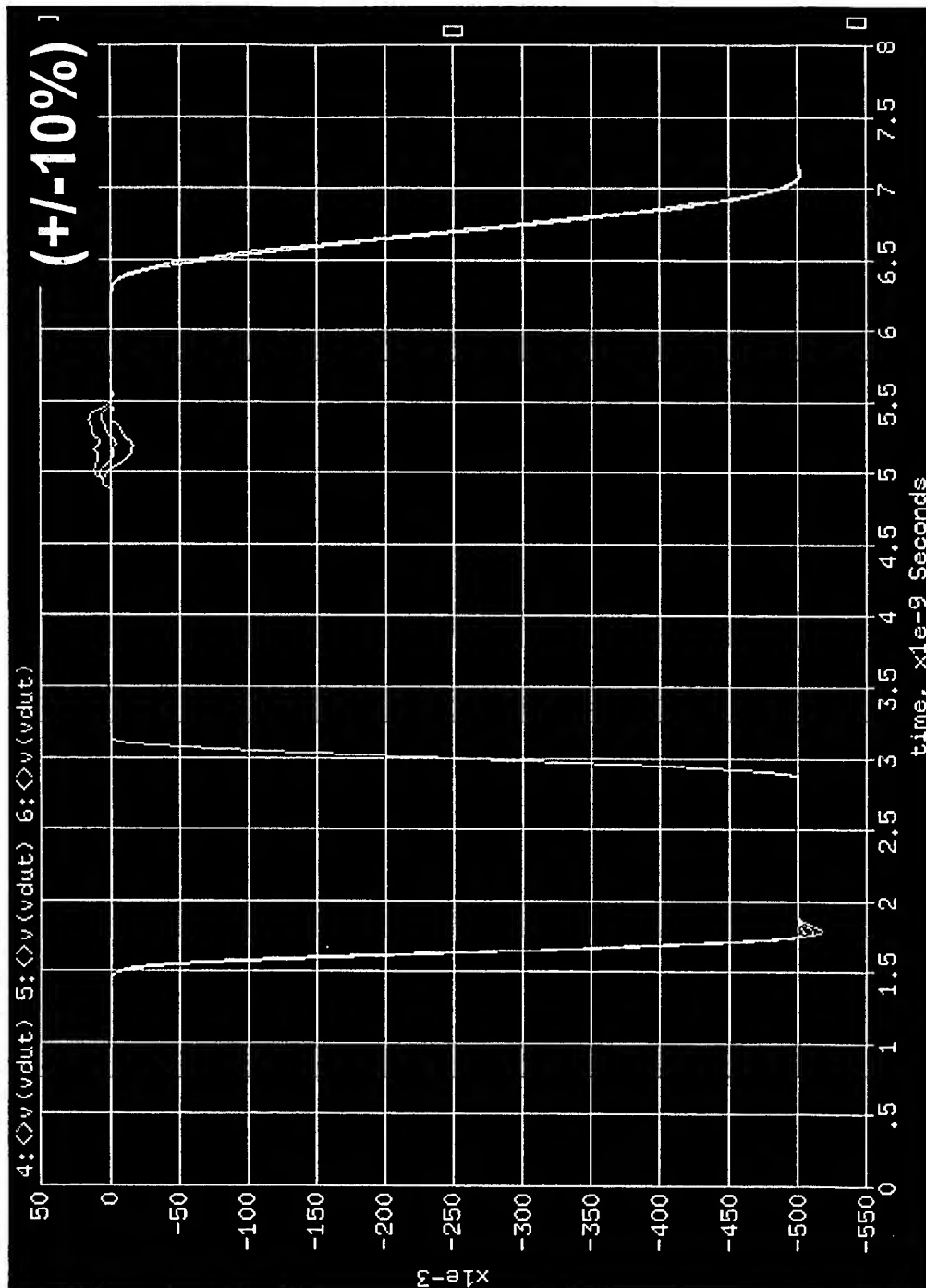
ADI Proprietary
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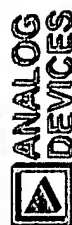


Sensitivity To Inductance Value

■ Composite Overview Waveform at DUT



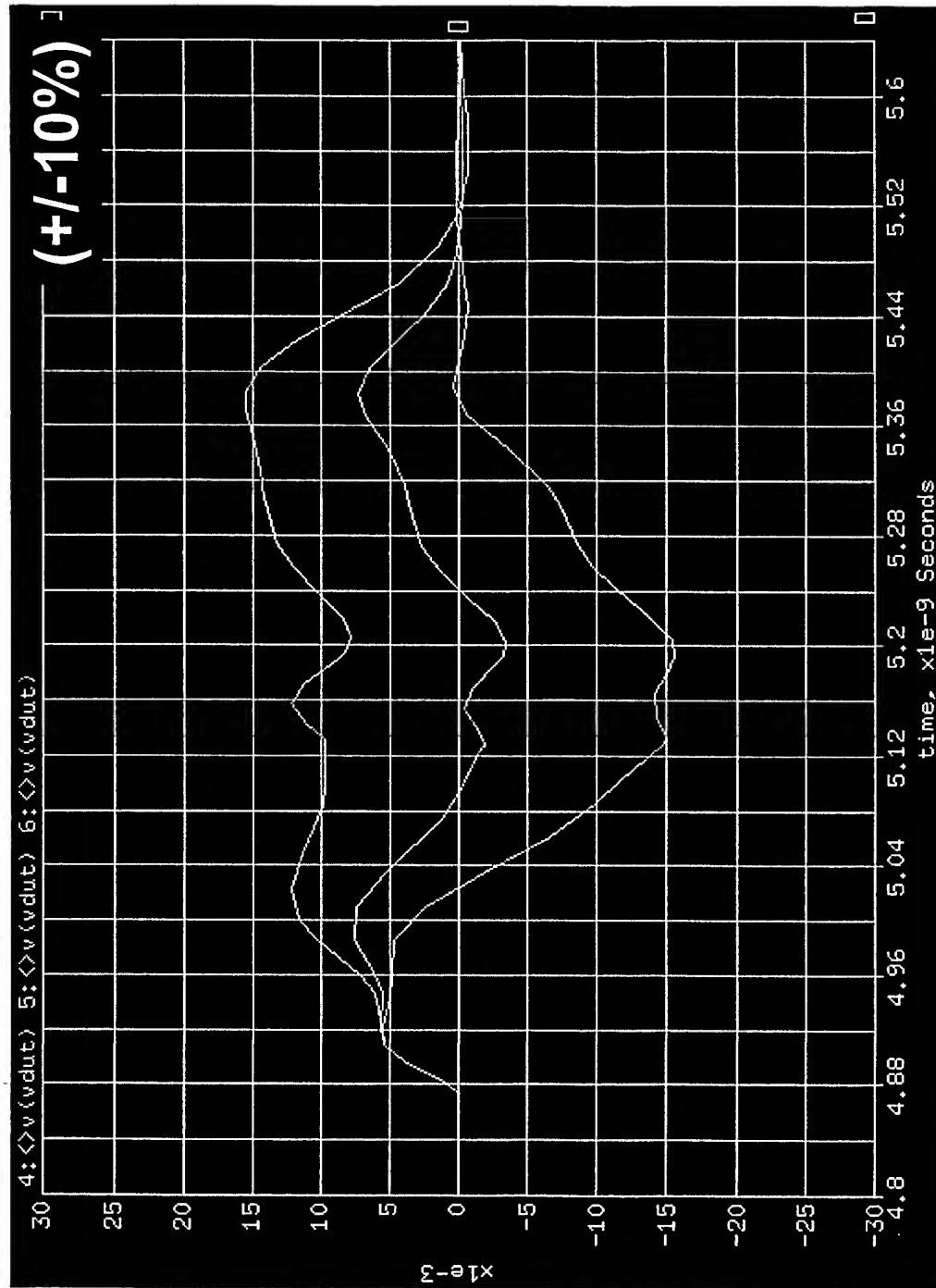
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Sensitivity To Inductance Value

Composite Overview Waveform at DUT - Reflection



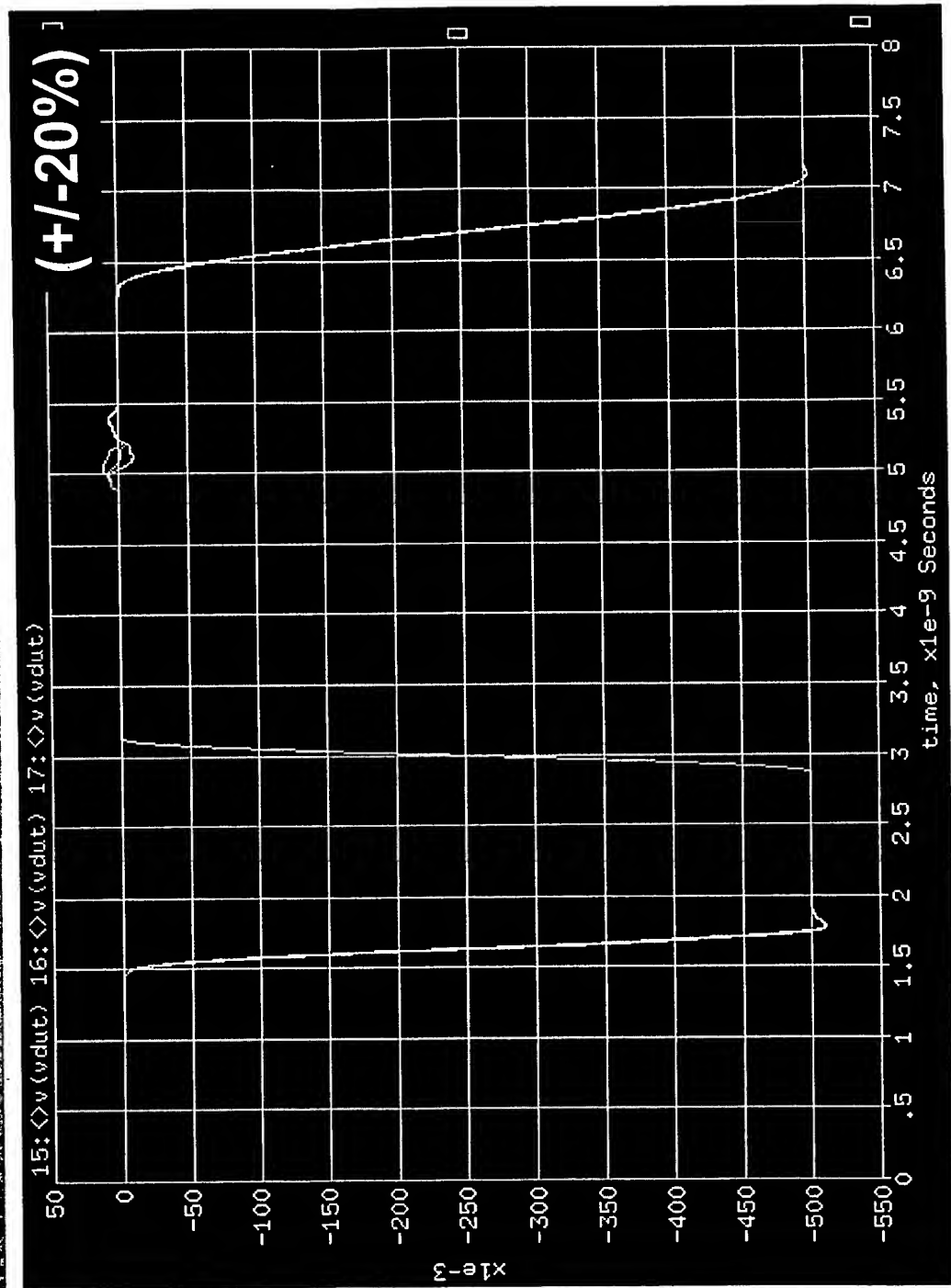
ADI Proprietary
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Sensitivity To Comparator Capacitance

■ Composite Overview Waveform at DUT



ADI Proprietary

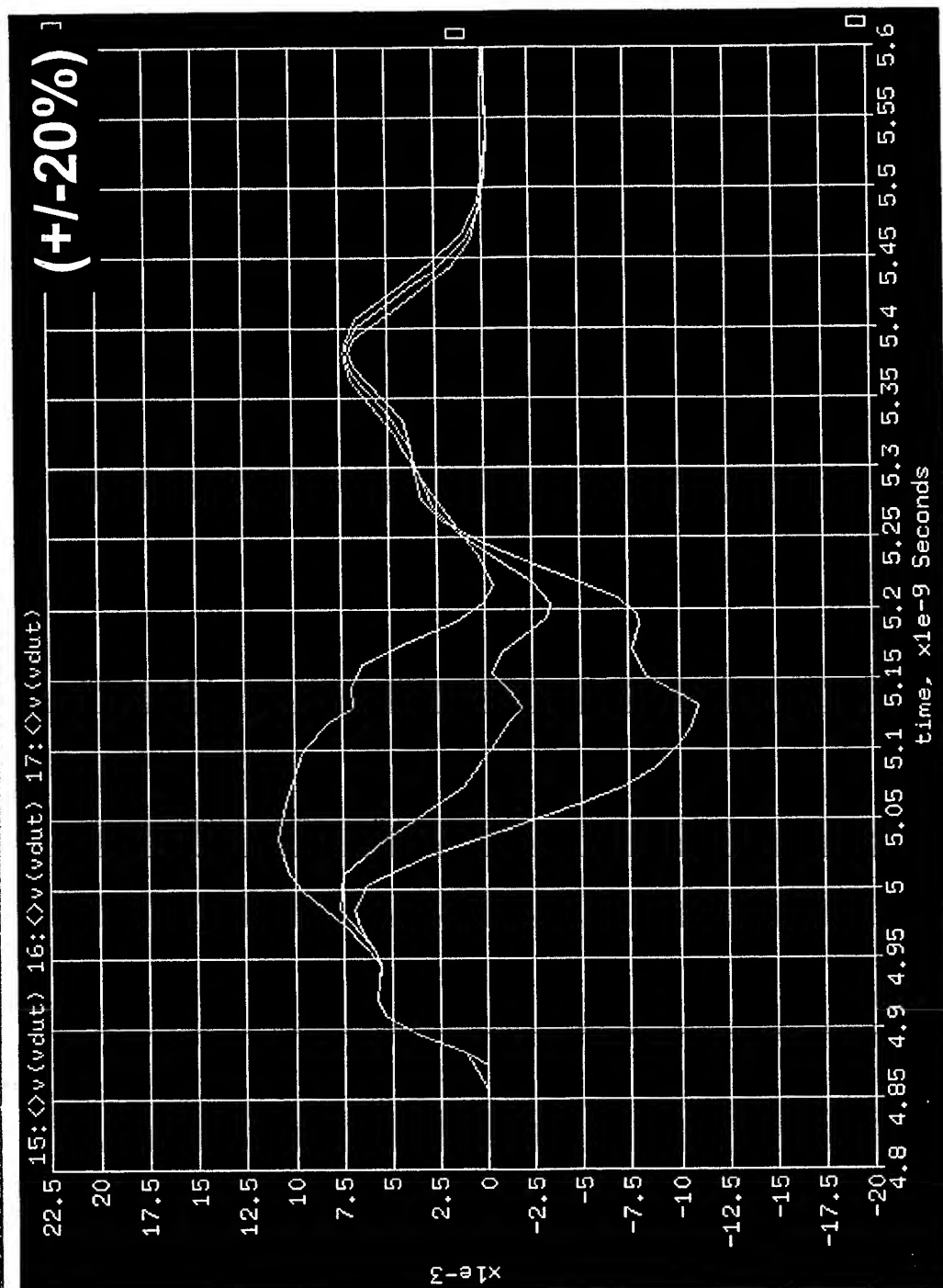
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Sensitivity To Comparator Capacitance

- Composite Overview Waveform at DUT - Reflection



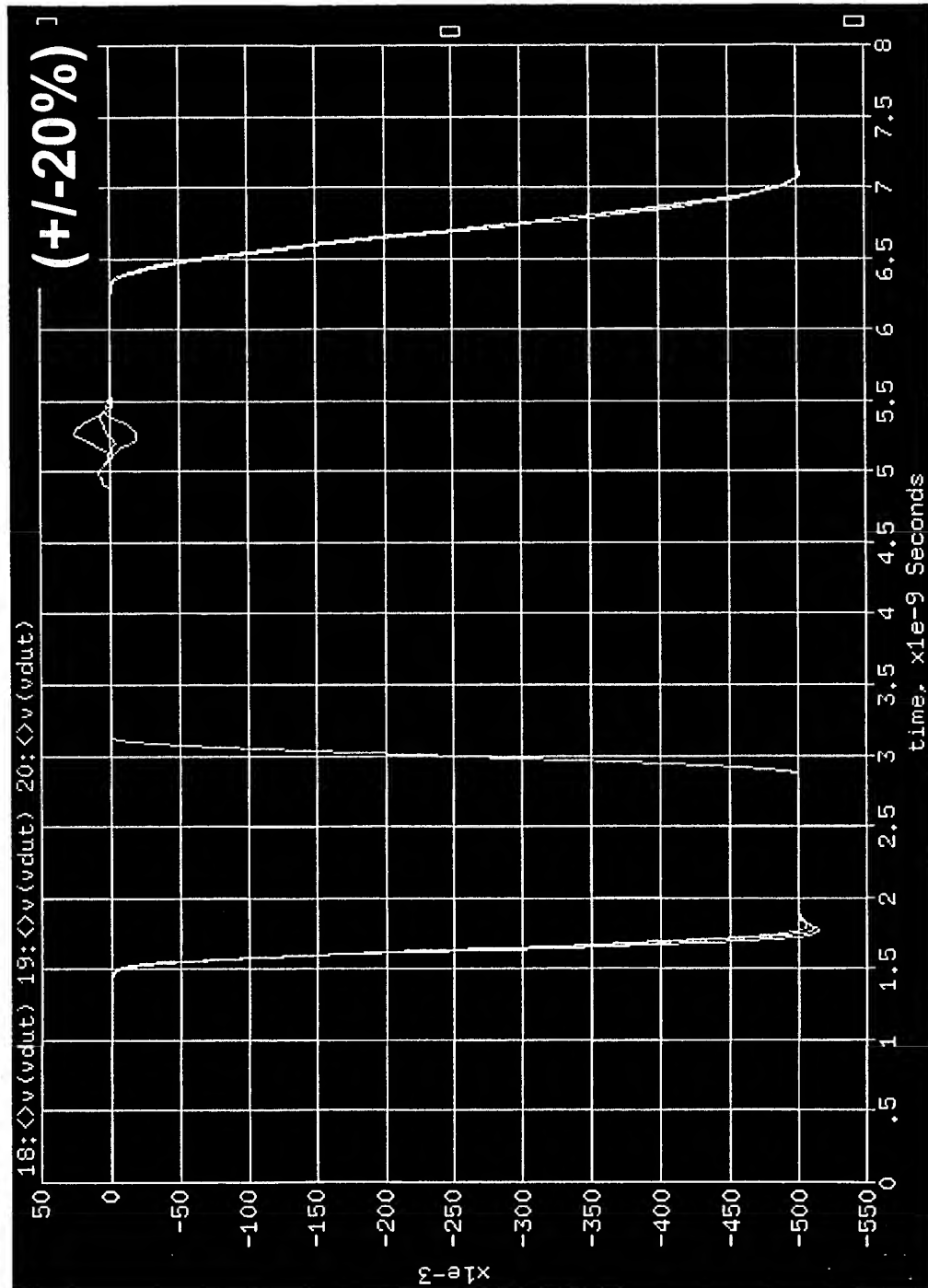
ADI Proprietary
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Sensitivity To A-Driver Capacitance

Composite Overview Waveform at DUT

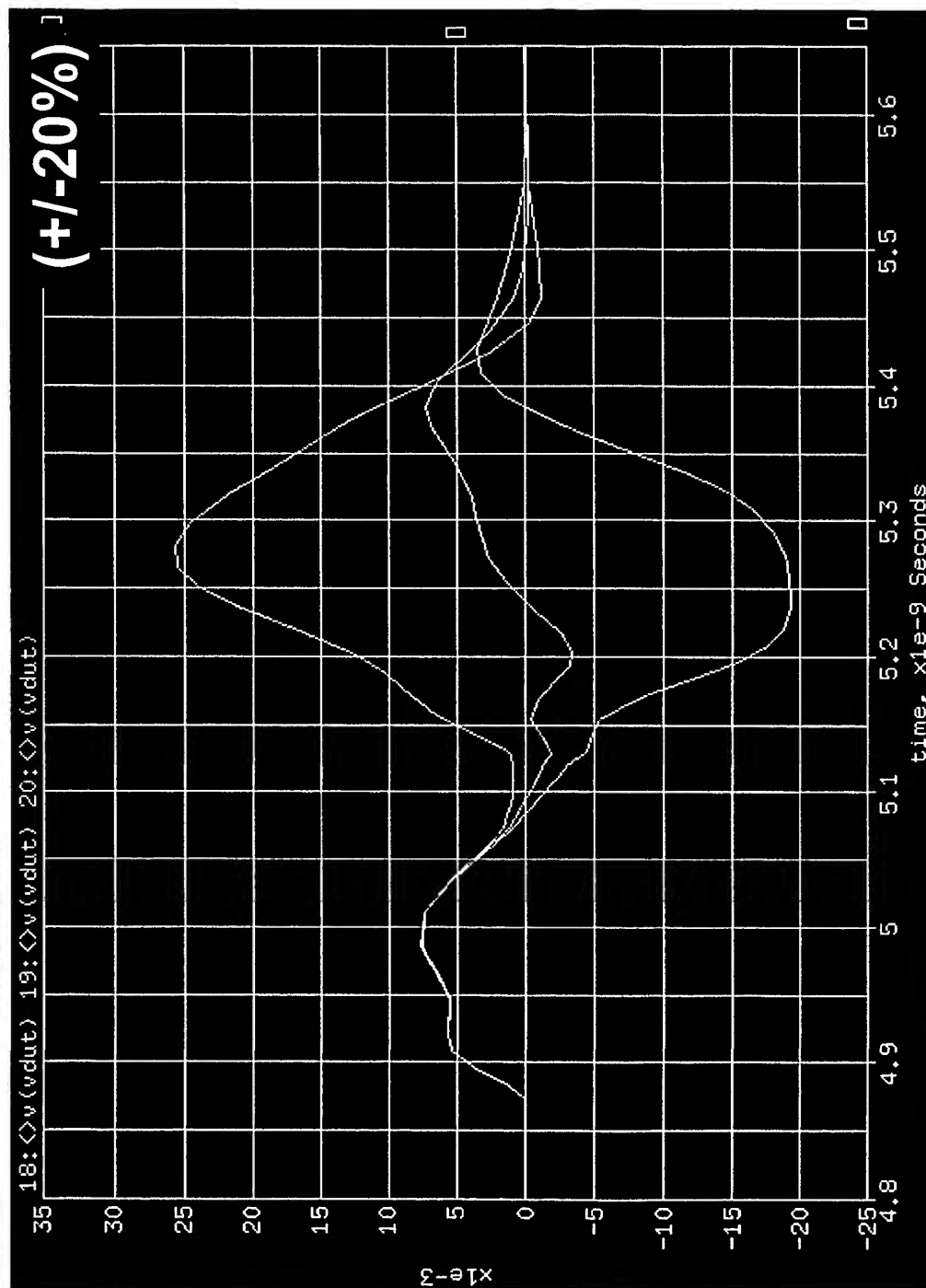


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Sensitivity To A-Driver Capacitance

- Composite Overview Waveform at DUT - Reflection



ADI Proprietary

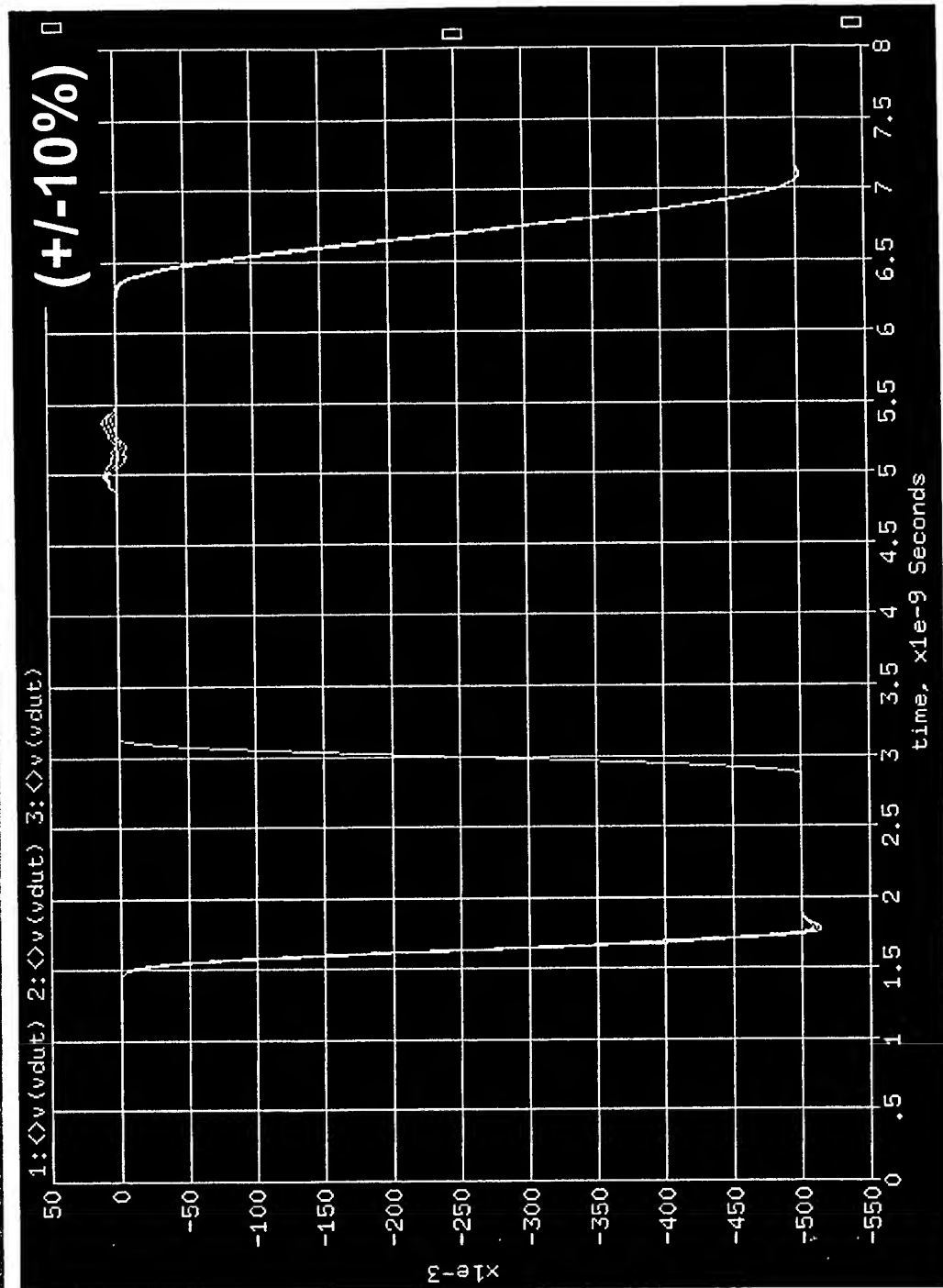
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Sensitivity To Parasitic Capacitance

■ Composite Overview Waveform at DUT



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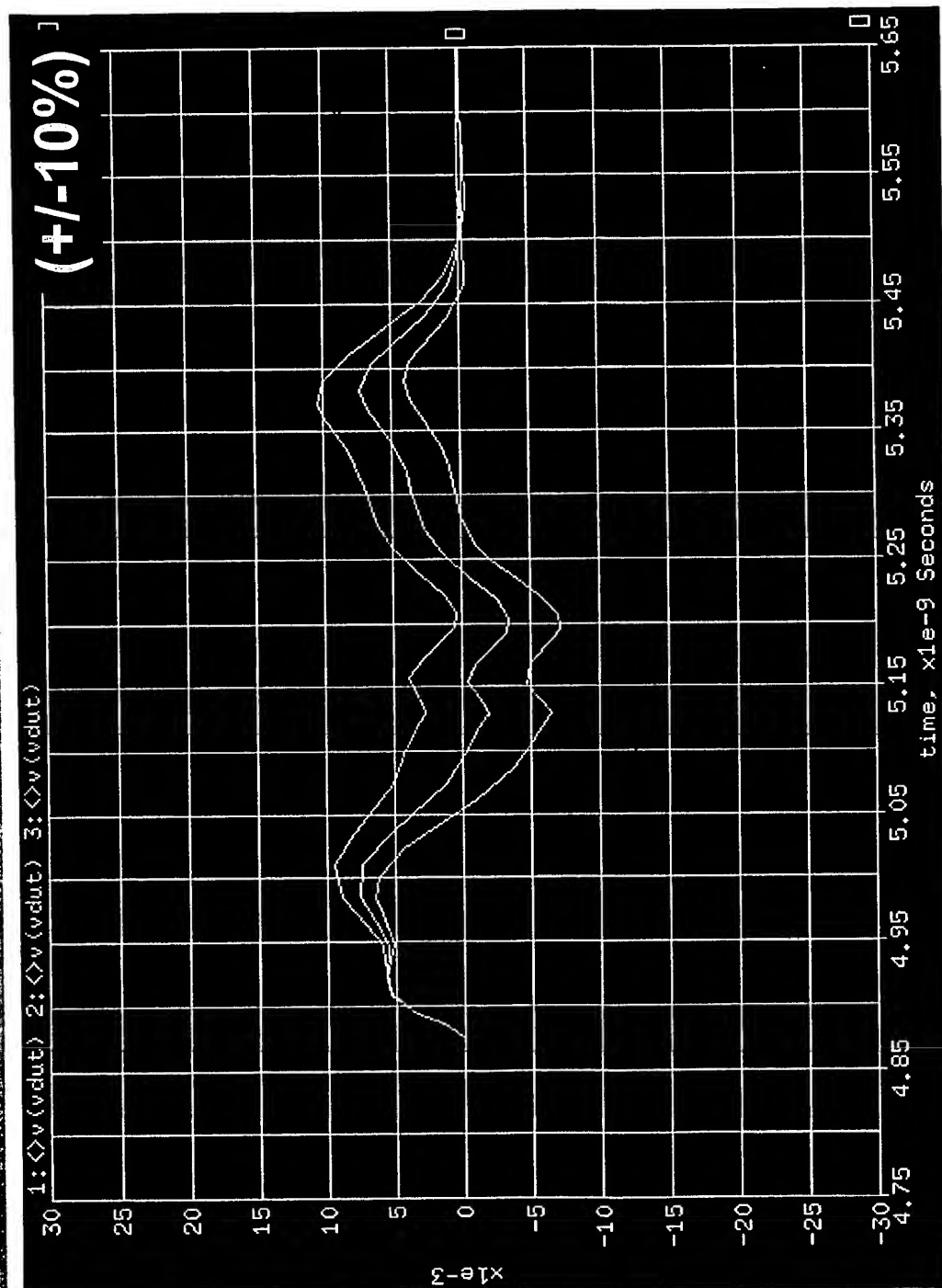
32

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Sensitivity To Parasitic Capacitance

Composite Overview Waveform at DUT - Reflection



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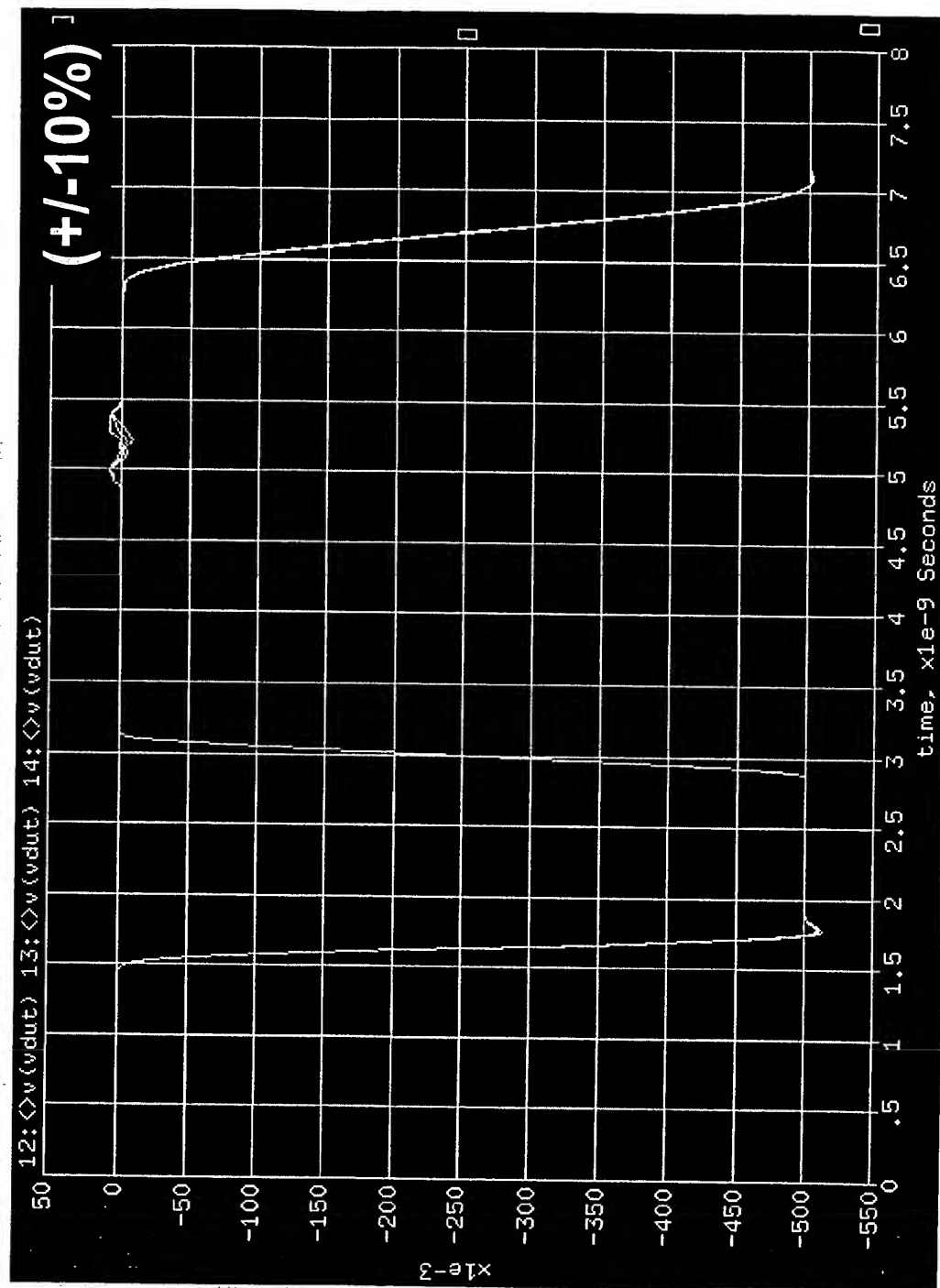
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Sensitivity To Coupling Coefficient

■ Composite Overview Waveform at DUT



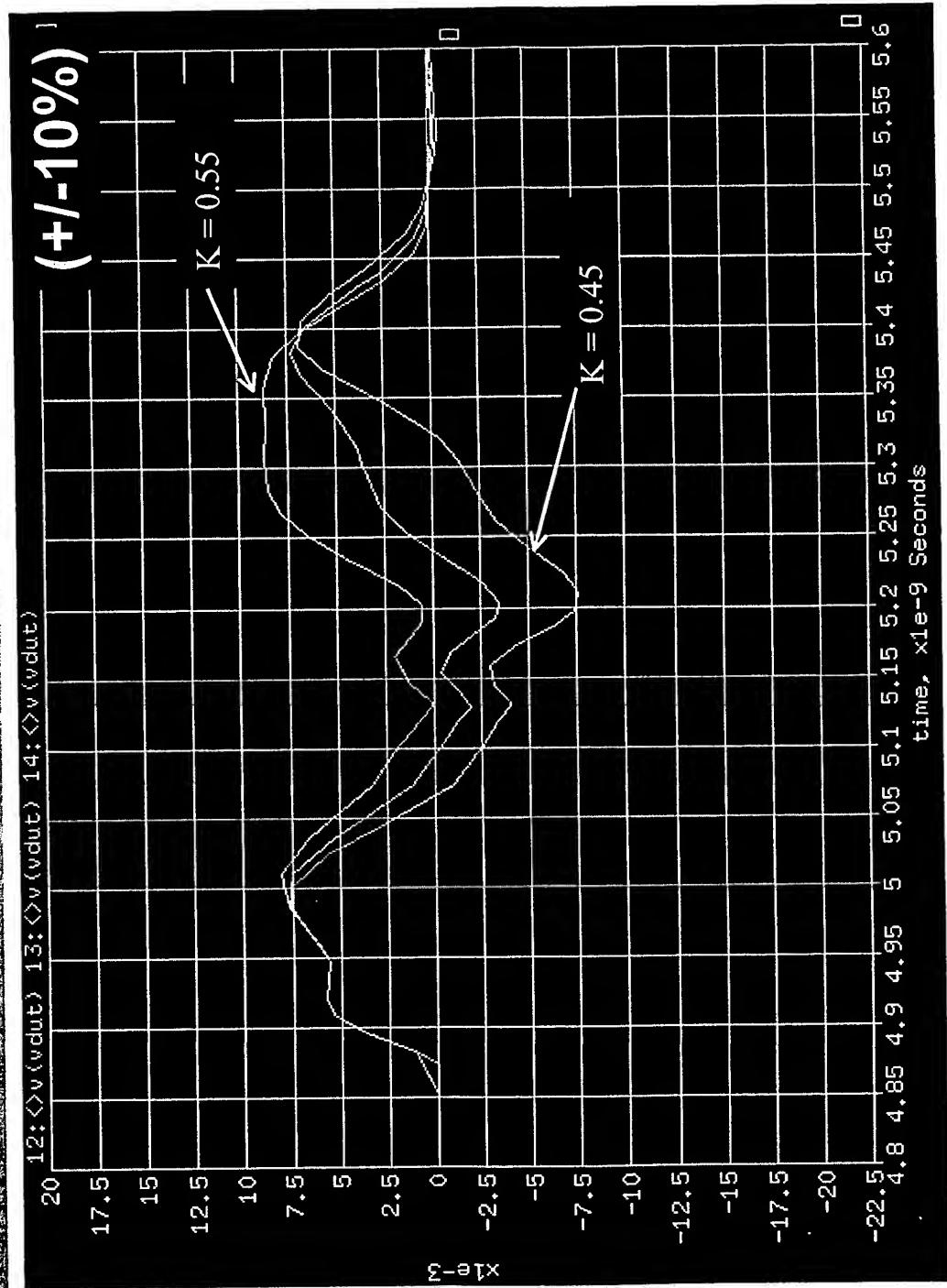
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Sensitivity To Coupling Coefficient

Composite Overview Waveform at DUT - Reflection

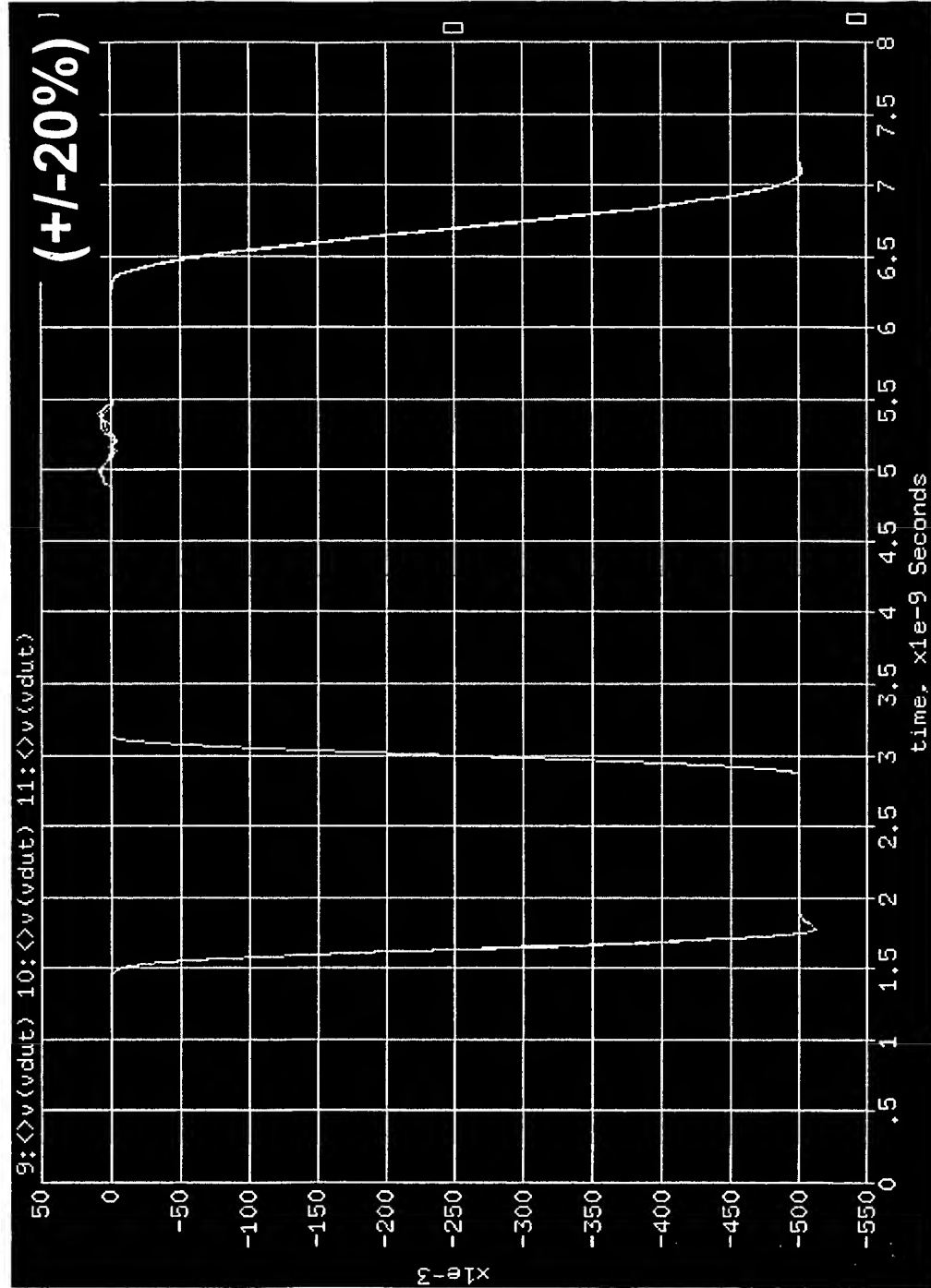


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Sensitivity To Bridge Capacitor Value

Composite Overview Waveform at DUT



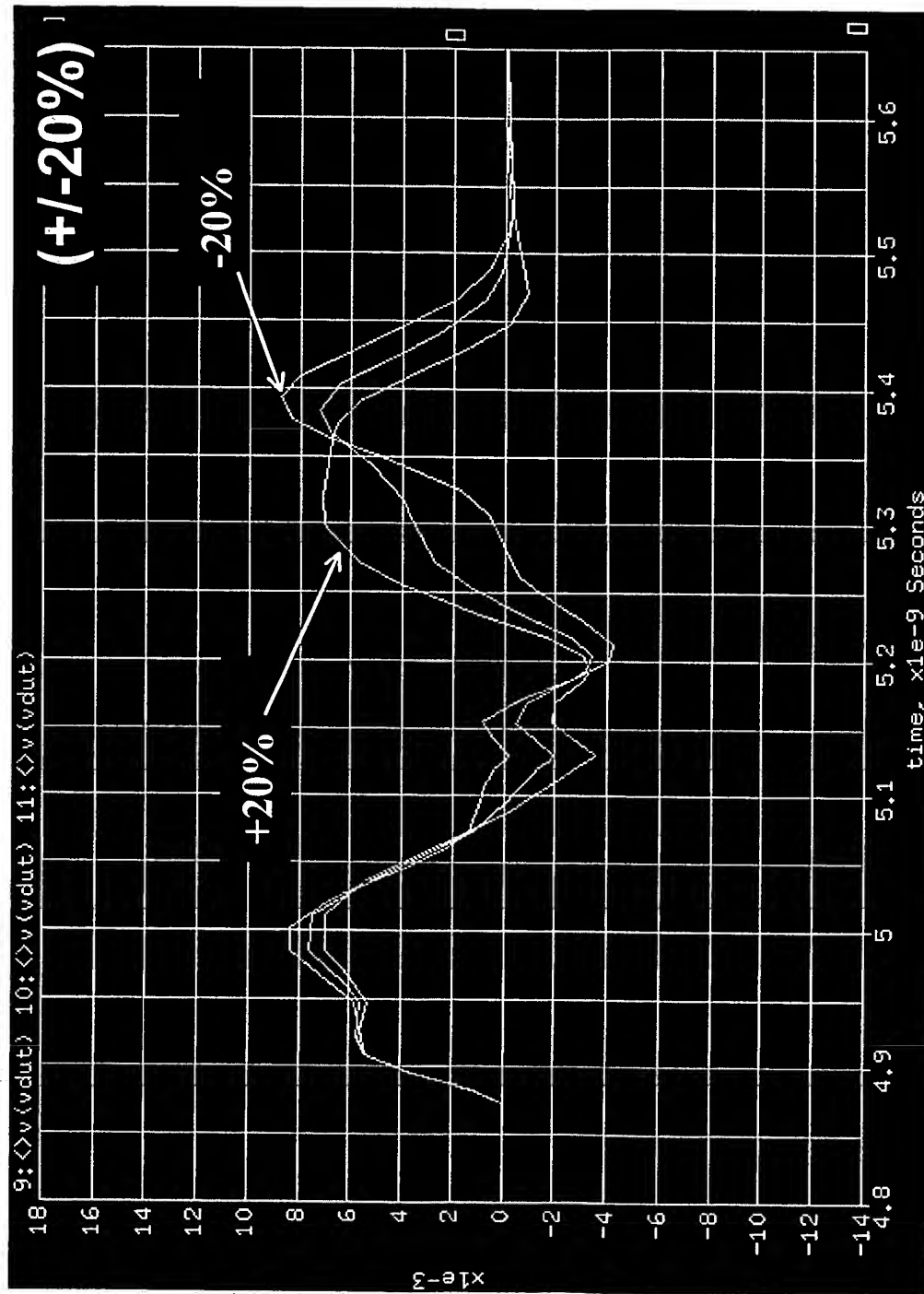
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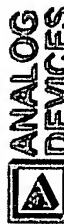
Sensitivity To Bridge Capacitor Value

- Composite Overview Waveform at DUT - Reflection



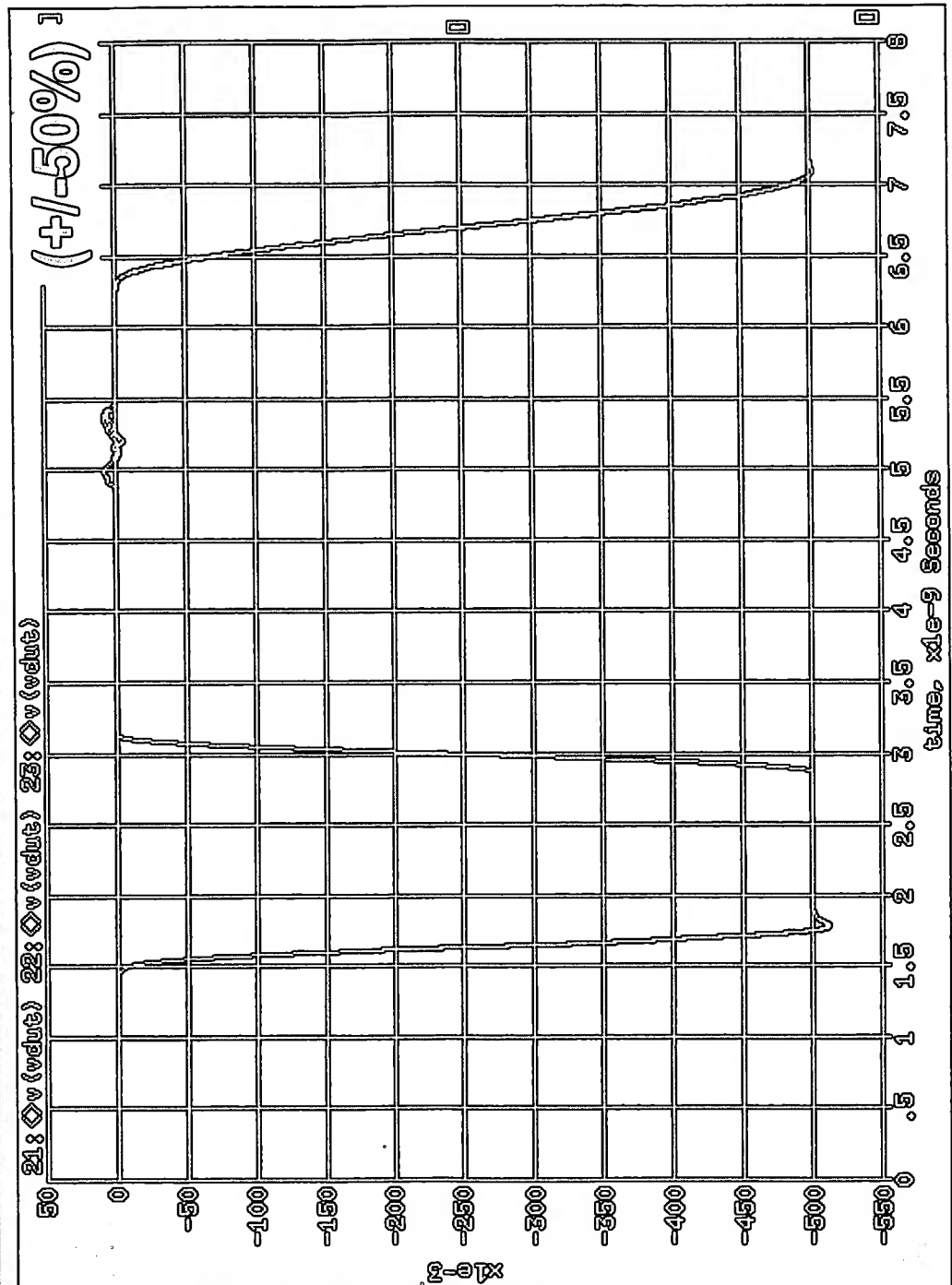
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Sensitivity To Coil And Trace Resistance

■ Composite Overview Waveform at DUT



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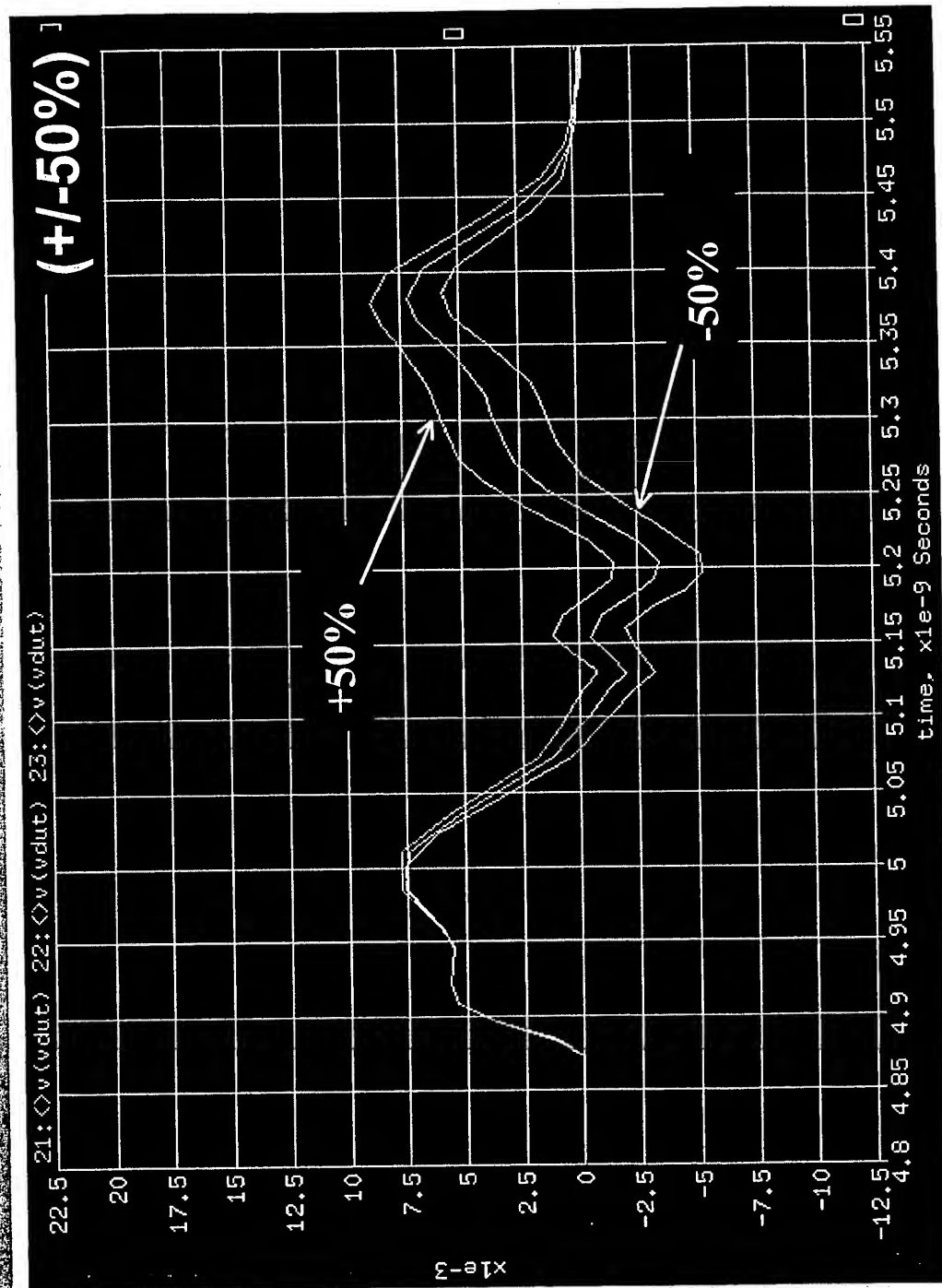
38

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Sensitivity To Coil And Trace Resistance

Composite Overview Waveform at DUT - Reflection



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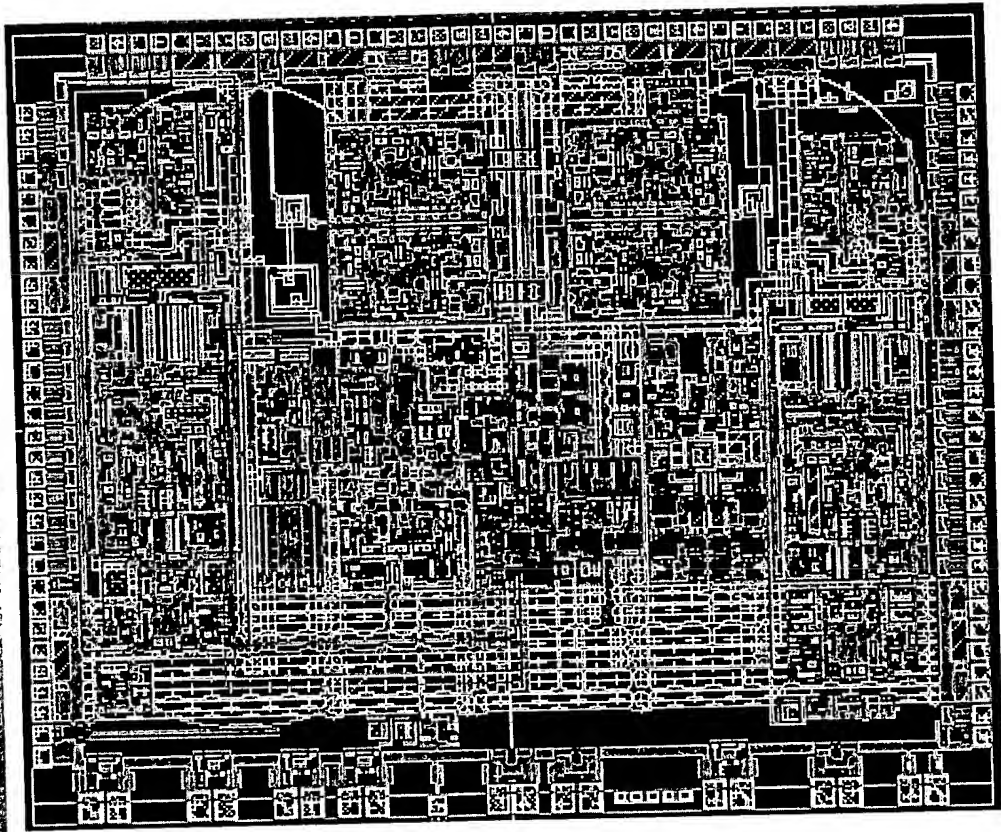
39



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Chip Layout Overview

- Preliminary - Work in Progress

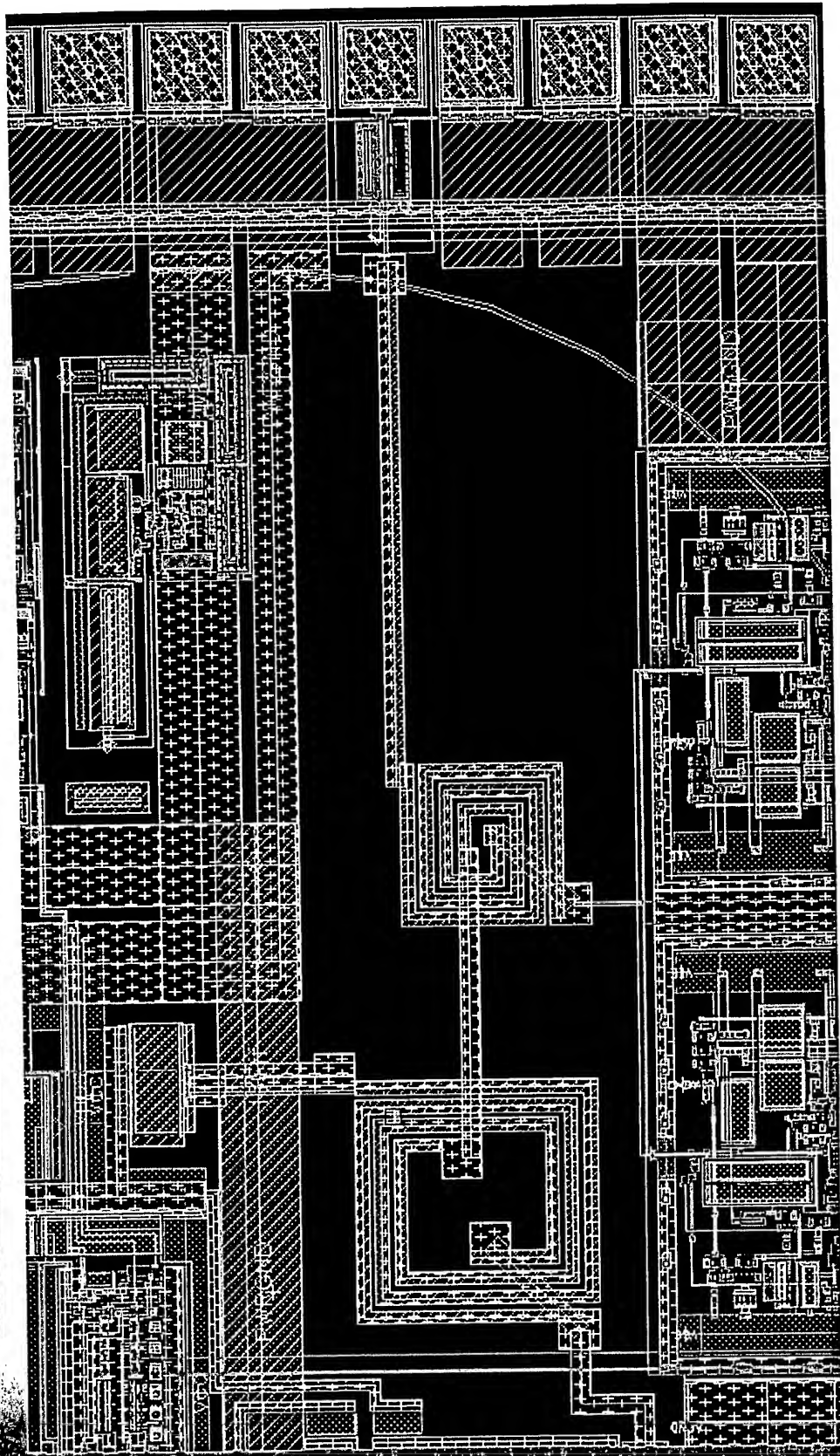


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Chip Layout: T-Coil Area Enlarged

■ Preliminary - "Artist's Conception" of T-Coils

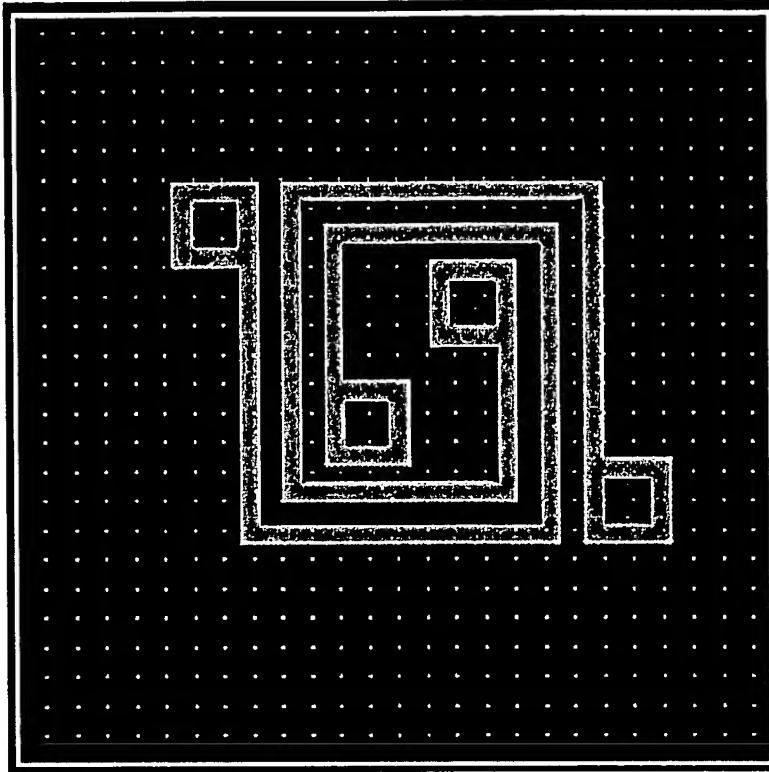
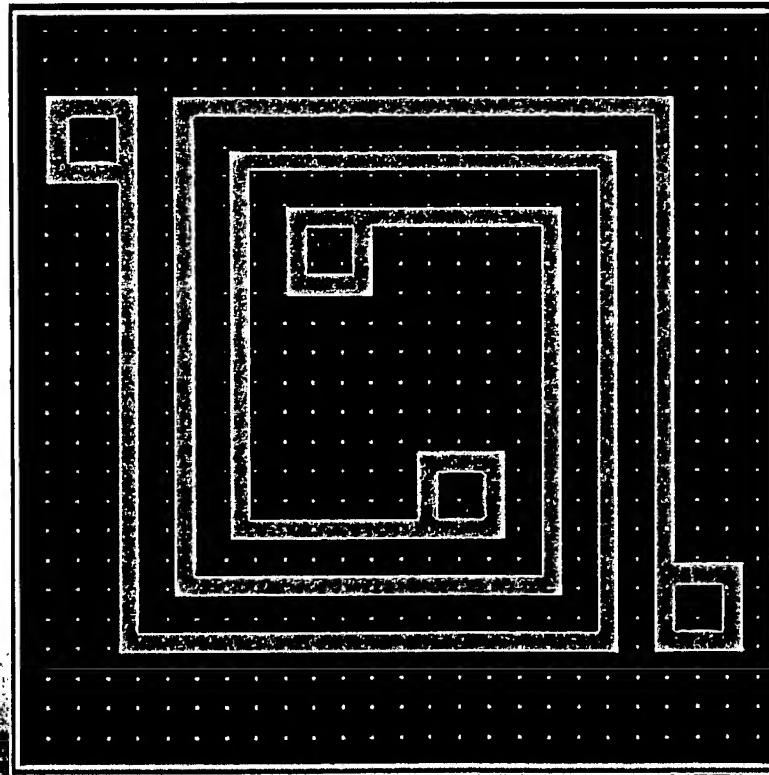


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Preliminary Actual Coil Layouts



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Where To Go From Here

- Finish Chip Layout
- Recalculate Values Based On Final Layout - Adjust Values As Required
- FAB IC
- Post-Process Coils At Multiple Suppliers
- Verify Models Through Characterization Of IC
- Gather Data For Process Spread Analysis
- Verify Reliability Through Qualification Process

Thanks To.....

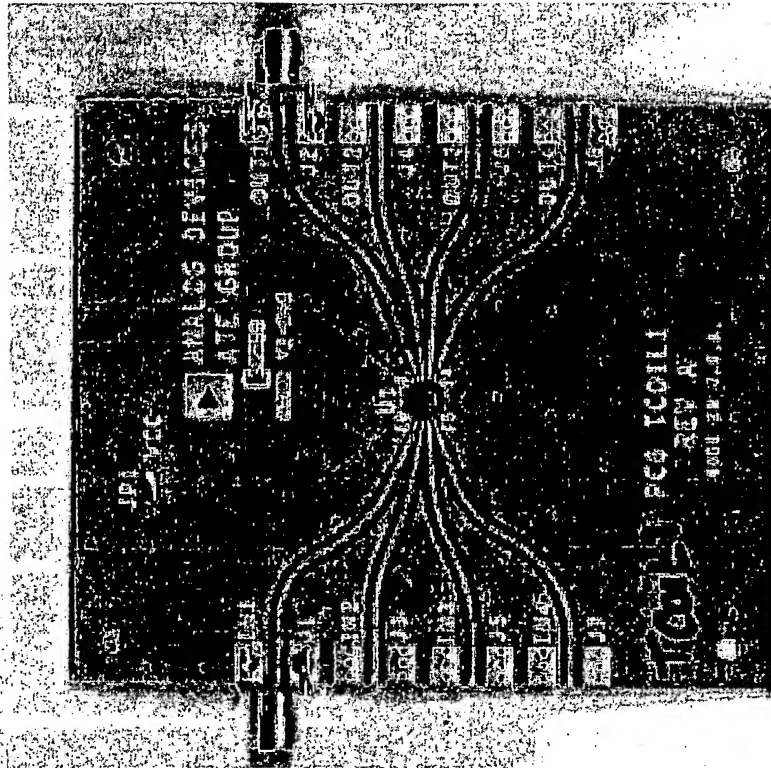
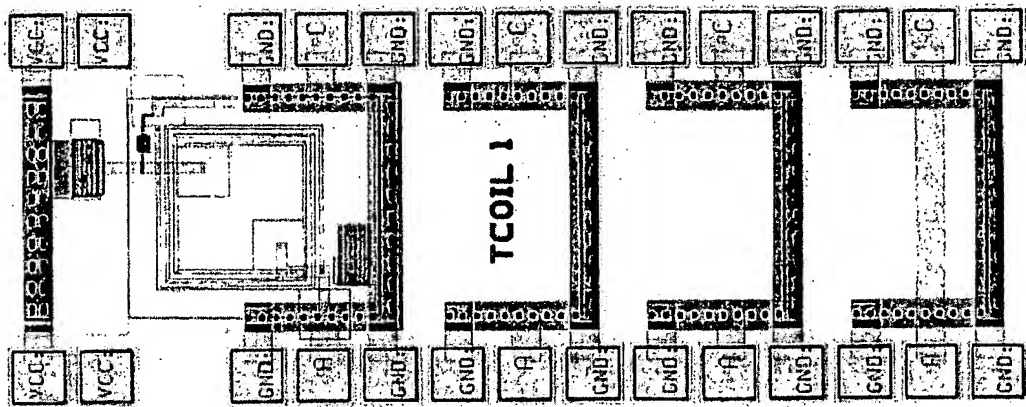
- Doug Babcock

- For the Original Ideas And Experience With T-Coils

- The UMIC Group

- For Continued Support And.....
 - Letting Us Believe It May Actually Be Possible

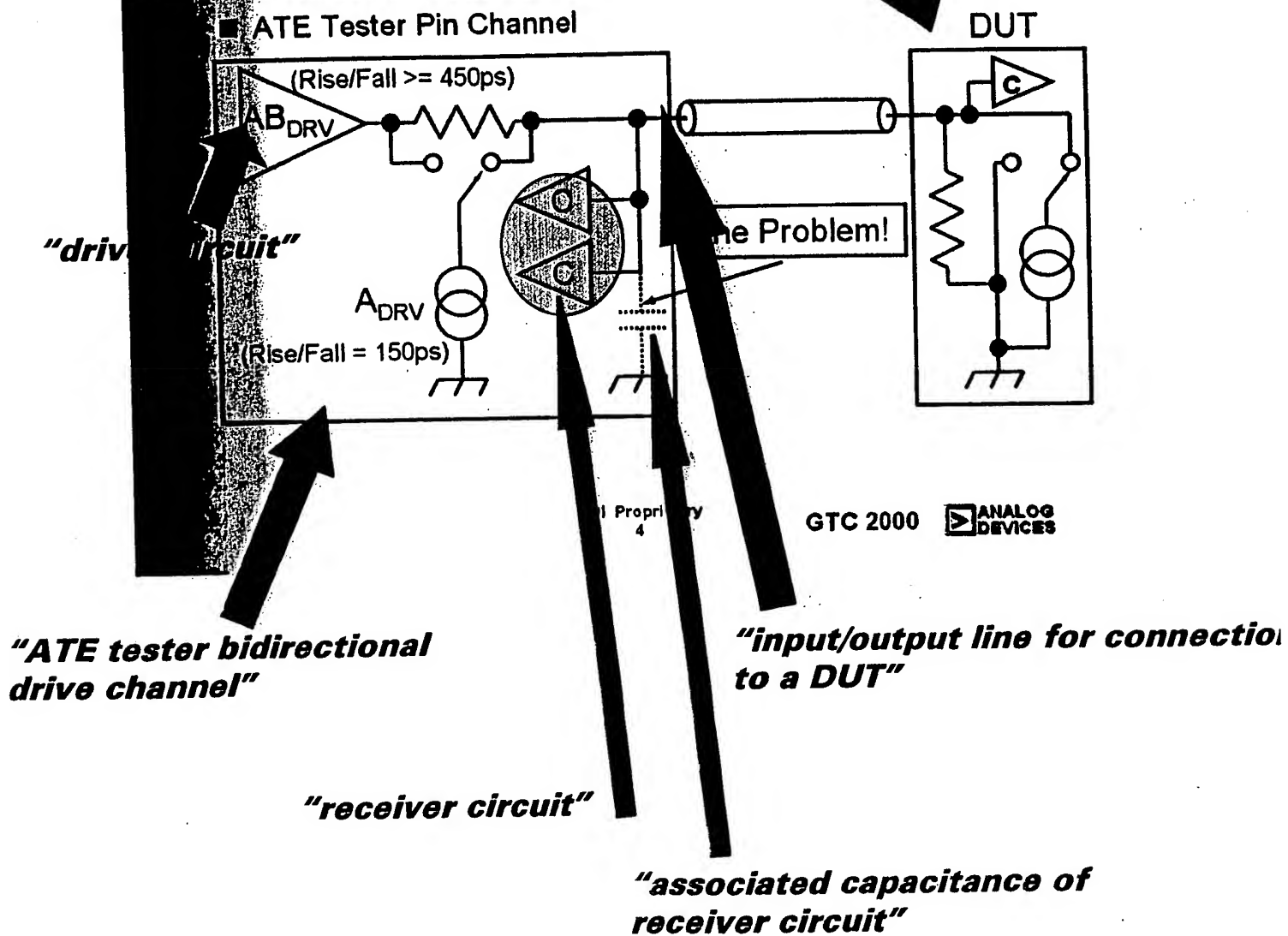
METAL 3 INDUCTOR / TCOIL STUDY



Boards: Bob Bombara
 Build: John Dixon
 Bonding: Rick Sullivan
 Layout: Jack Mason, Joe Zagami
 GTC 2000

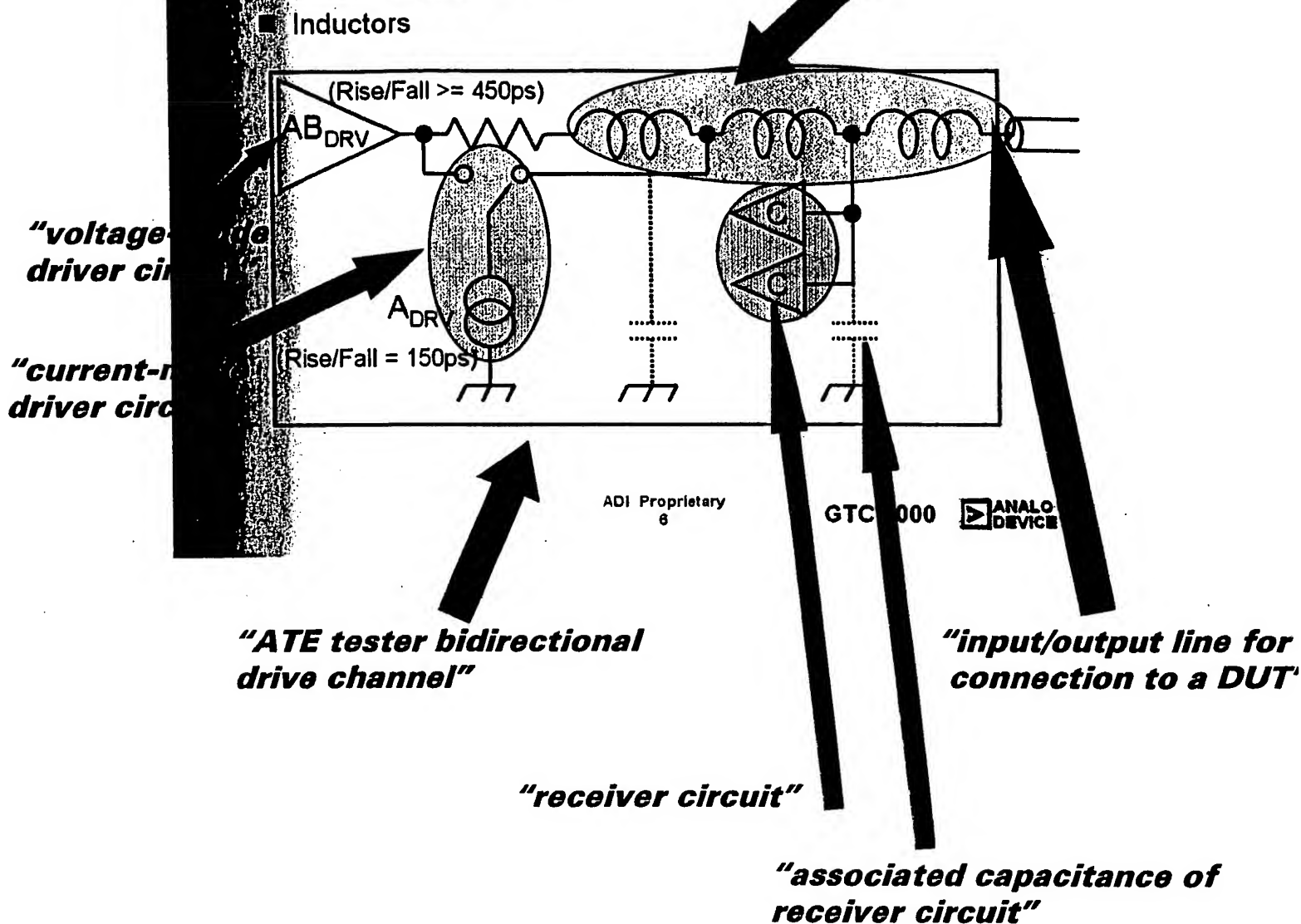
"DUT = Device Under Test"

What problem are we trying to solve?



How Do We Compensate

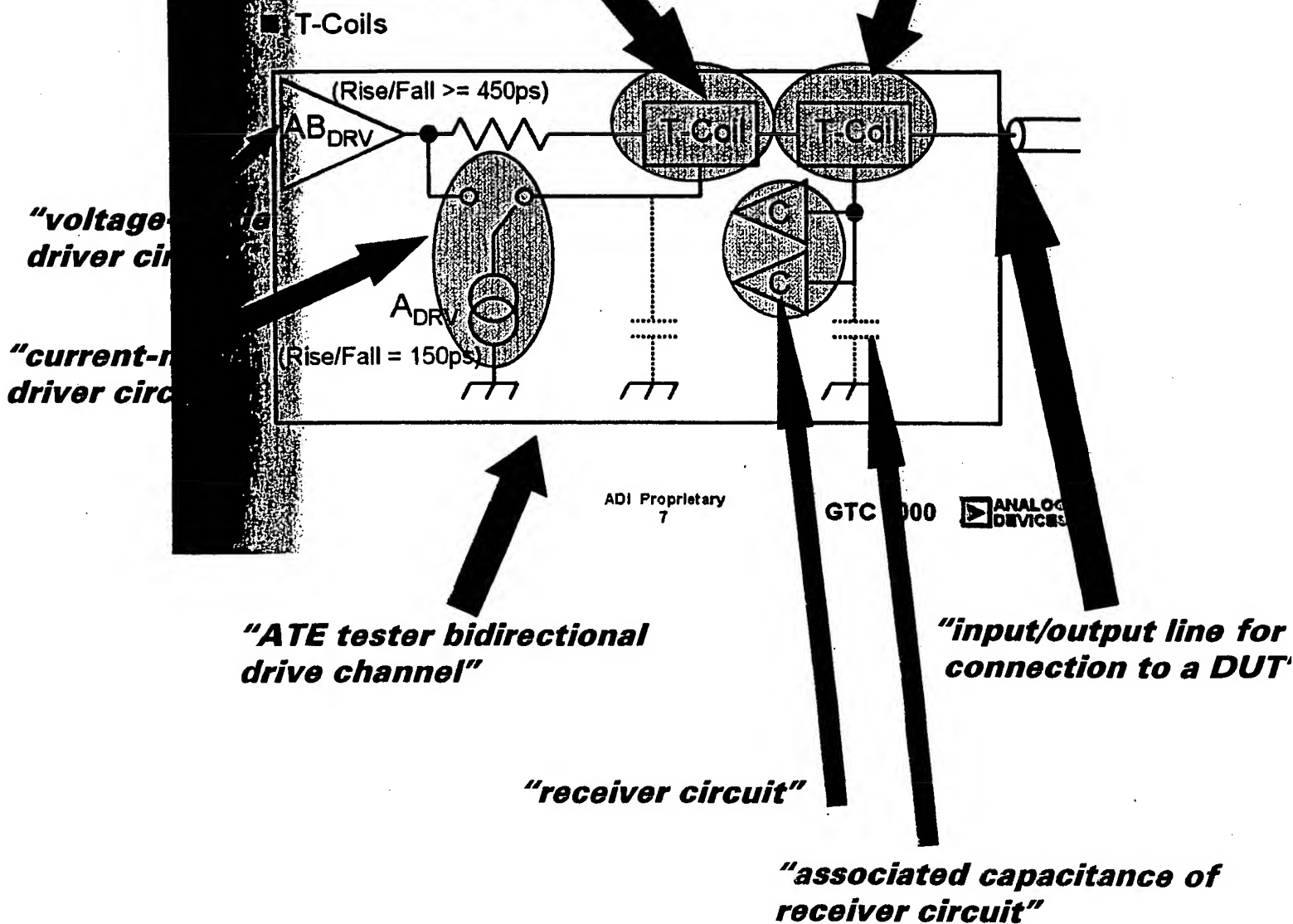
"first passive matching network to at least partially compensate for receiver circuit capacitance"



"second passive matching network, comprising a T-Coil circuit, compensating for current-mode driver capacitance"

"first passive matching network comprising a T-Coil circuit, compensating for receiver capacitance"

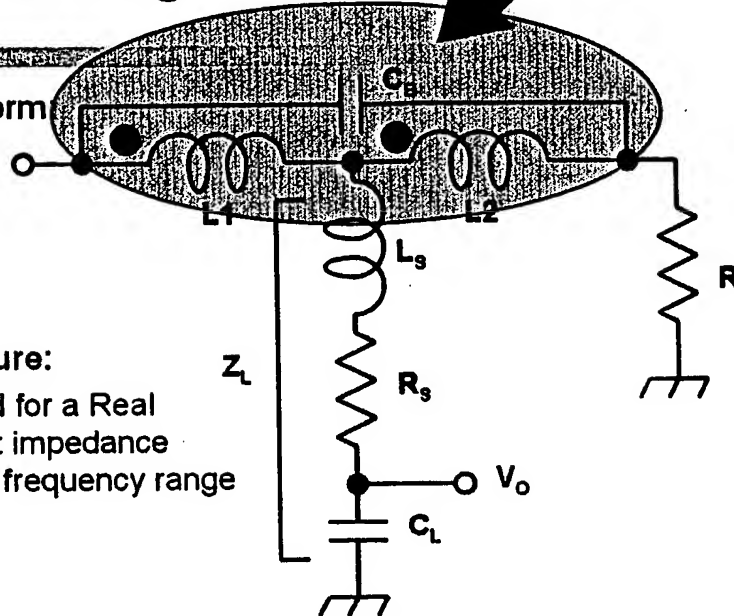
How Do We Compensate?



*"first passive matching network,
comprising a T-Coil circuit"*

What is a Bridged T-Coil?

The General Form



Important Feature:

- ☐ Can be tuned for a Real 50-ohm input impedance over a broad frequency range

ADI Proprietary
2

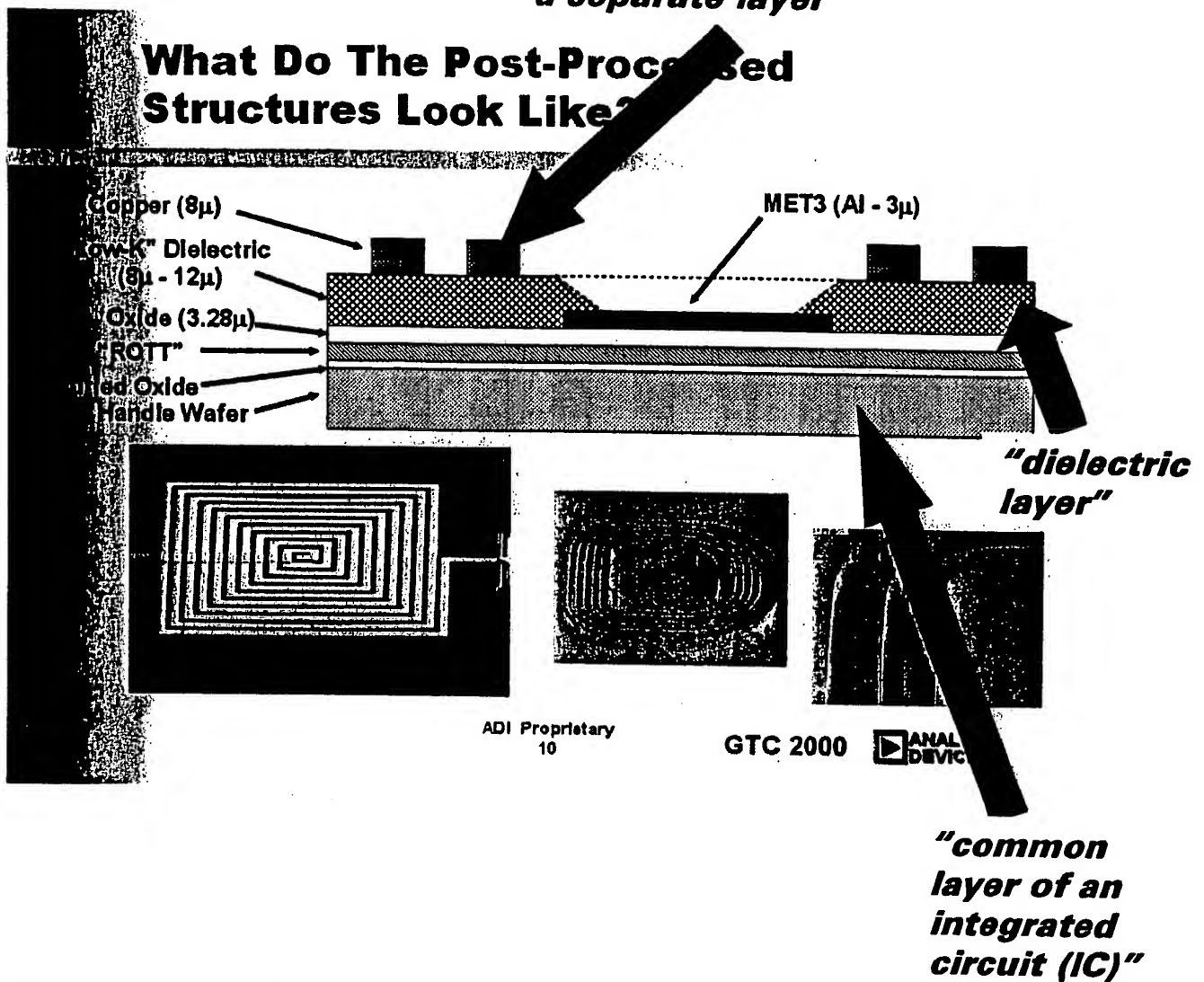
GTC 2000 

The T-coil circuit is formed by the transformer coupled-inductors, L1 and L2. The dots to the left of the coil symbol indicate the magnetic flux through the coils are linked in the polarity indicated. C_B is the bridging capacitor.

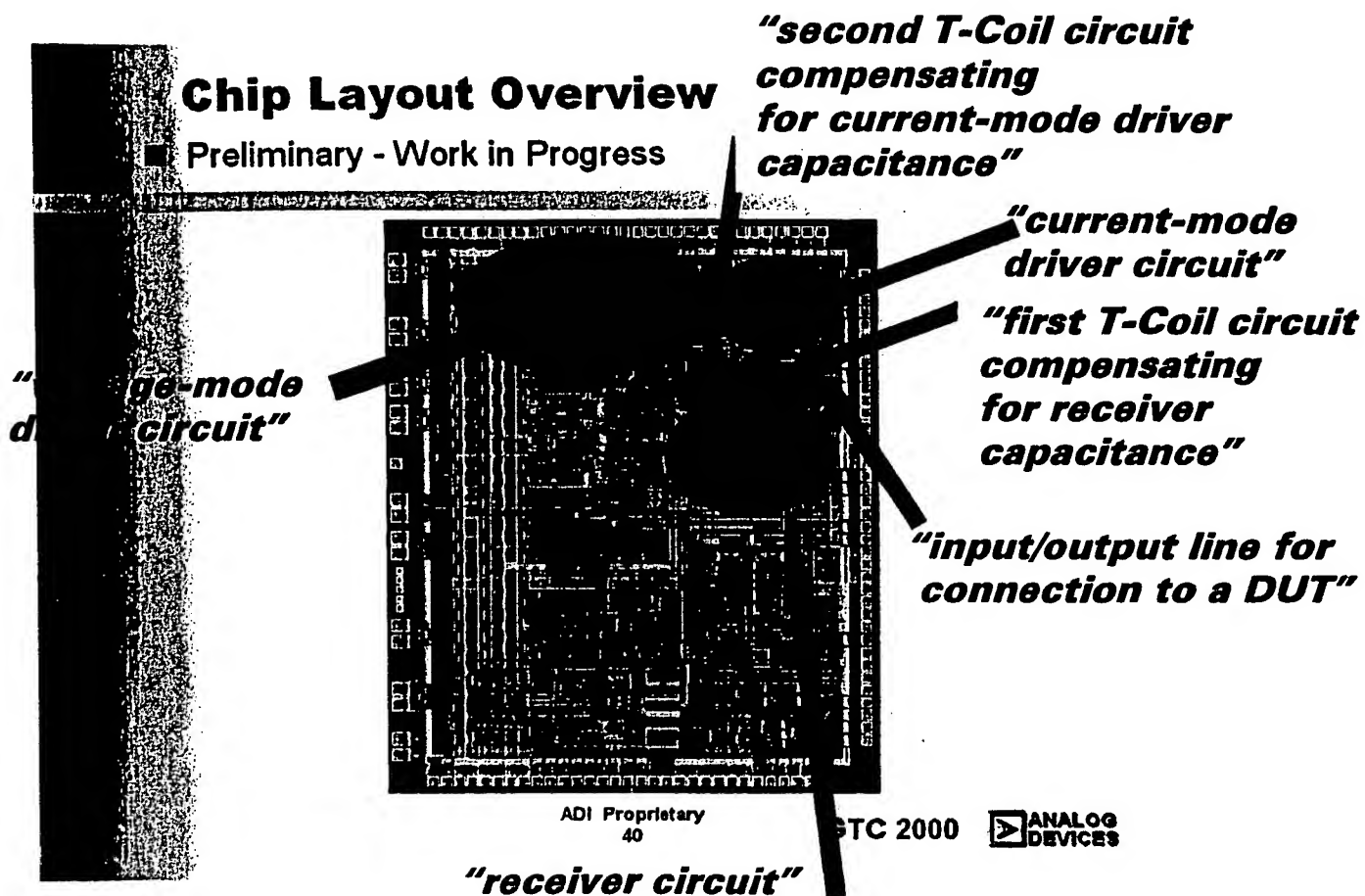
The elements L_S , R_S represent the circuit elements of series inductance and series resistance connecting the T-Coil circuit to the load capacitance C_L . In the case of the ATE Pin Electronics system, this could be the receiver associated capacitance.

"T-coil inductors implemented in a separate layer"

What Do The Post-Processed Structures Look Like?



Cross section showing T-Coil transformer coils implemented in a separate layer of an IC that is spaced from the common layer by at least a dielectric layer.



Integrated circuit layout plot showing driver, receiver, input/output line, and T-Coils.

***"first passive matching network,
comprising a T-Coil circuit,
compensating for receiver capacitance"***

***"current-mode
driver circuit"***

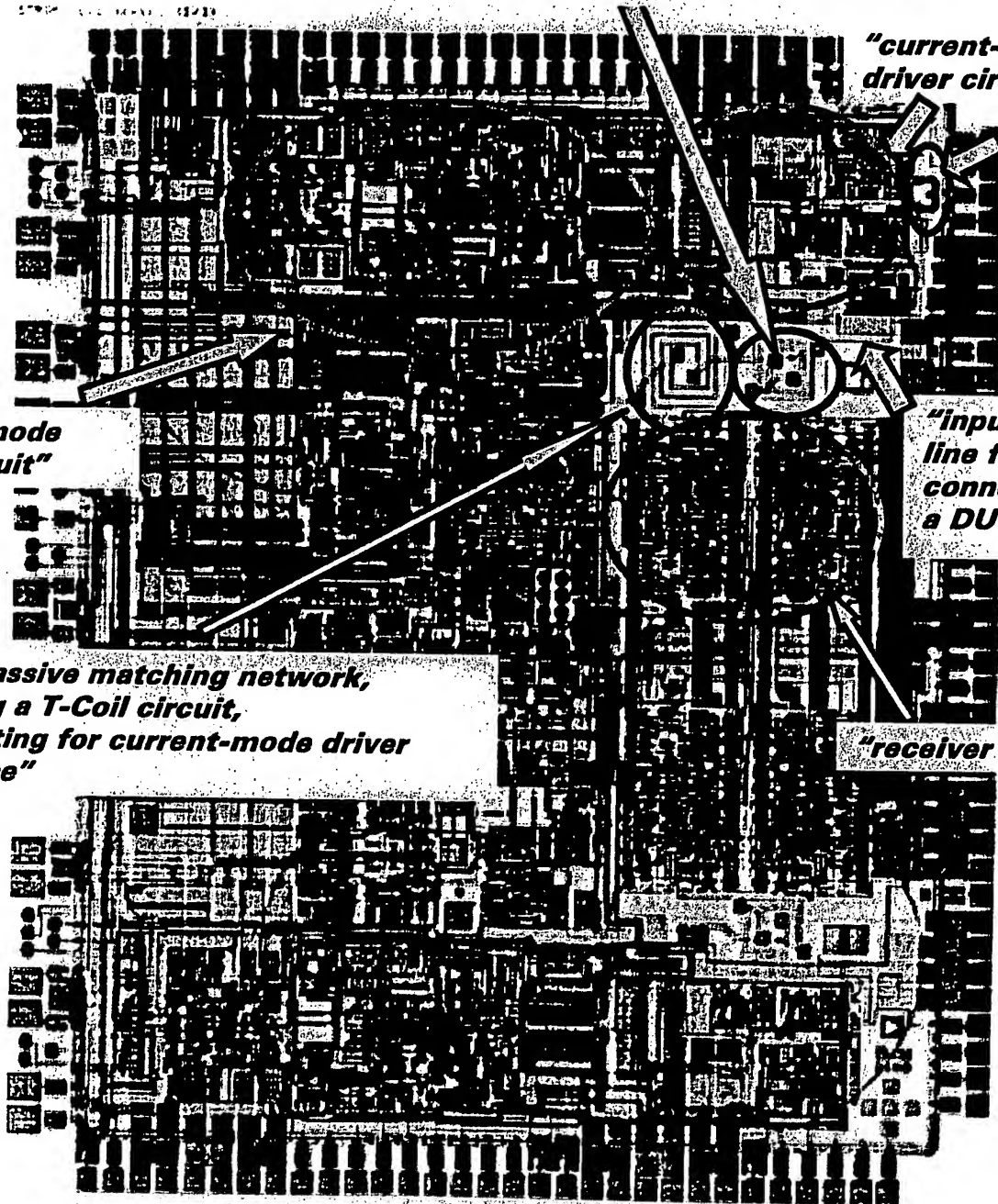
***"die label
version 3"***

***"voltage-mode
driver circuit"***

***"input/output
line for
connection to
a DUT"***

***"second passive matching network,
comprising a T-Coil circuit,
compensating for current-mode driver
capacitance"***

"receiver circuit"



***"first passive matching network,
comprising a T-Coil circuit,
compensating for receiver capacitance"***

***"current-mode
driver circuit"***

***"die label
version 4"***

***"voltage-mode
driver circuit"***

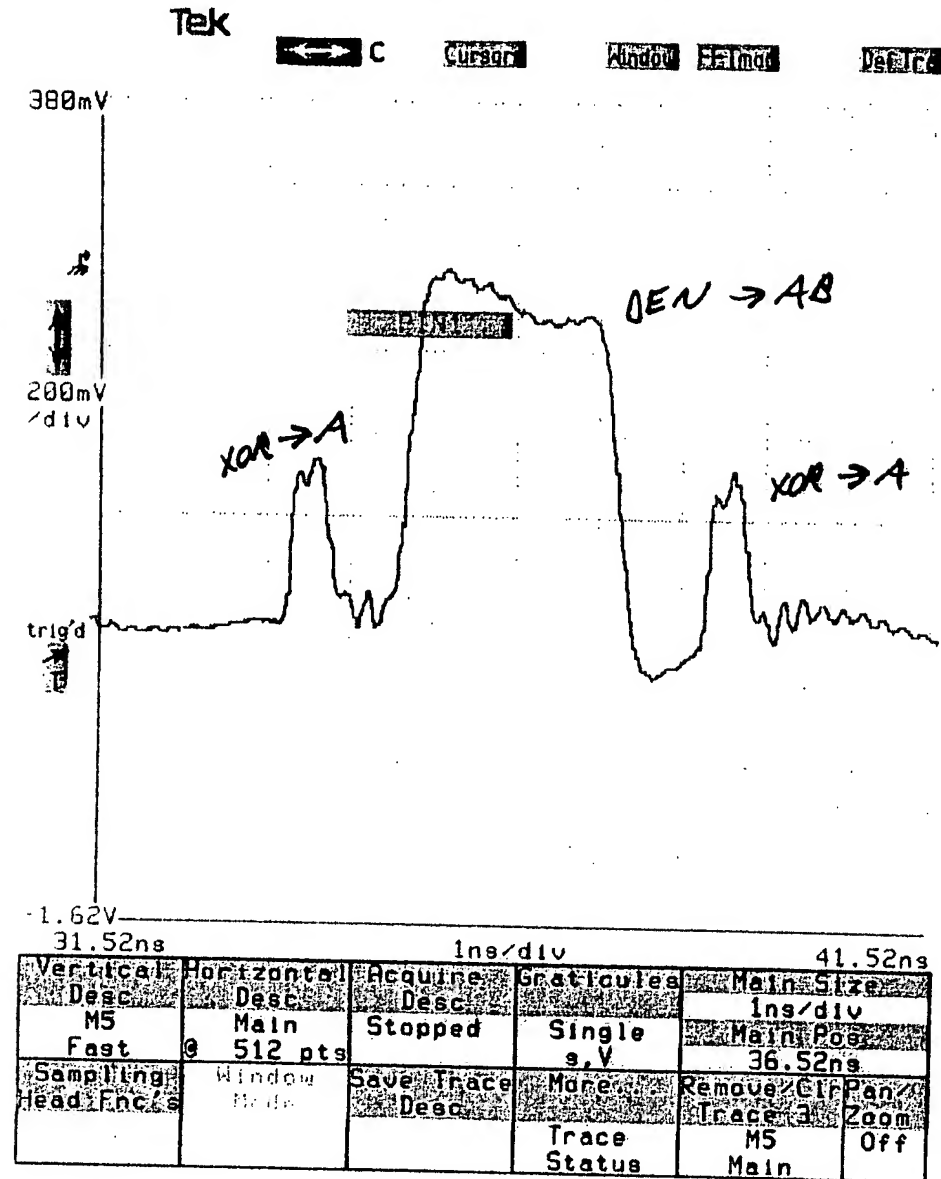
***"input/output
line for
connection to
a DUT"***

***"second passive matching network,
comprising a T-Coil circuit,
compensating for current-mode driver
capacitance"***

"receiver circuit"

Plot created by cad on 23 May 2000 (262515) using d051510_top_vary.gls
Top structure: d051510_top_vary Layers: 1-33, 15-18, 20-24, 26-32, 42-45, 47, 55, 58, 63
Hatched on: 1 Registered on: GABRI, Full: FIRM, Name:
Minlevel: 1-2210.001, 2615.000, 12210.000, 2615.000, 01e size: 4420.000 by 5350.000 at level 544161 45.00

11801C DIGITAL SAMPLING OSCILLOSCOPE
date: 22-AUG-00 time: 20:13:26



Measurement of functional operation of ad53510pc silicon, August 22, 2000
showing current-mode driver (A) and voltage-mode driver (AB) operation.

return/ad53510/6379805/read.me

First Samples Ad53510-PC

Wafer 637980-5

Trimmed 20-Sep-2000

Program is archived in

doc: /cts5000/home/eng/ad53510_archive/1stSample_092000
alltestcode_1stSample_092000.tar.Z

637980_5_ad53510PC_trm_doc_092000_184151.stdf

Site 1 Version 0 Yield 8/24

...Tweaked SLRD trim geometry, opened up test limits to improve yield.

637980_5_ad53510PC_trm_doc_092000_182850.stdf

Site 2 Version 0 Yield 15/20

Die stepping misaligned because find_first_die targets
in vs_align2.dat were incorrect; first 9 tested were all bin-1's
but were not marked because gv_trm_scratch_pad was off;
walked off wafer after #20, then program crashed & needed ^X;

637980_5_5_ad53510PC_trm_doc_092000_181452.stdf

Site 2 Version 0 Yield 2/3

Manually wrote to scratchpad 1st 9 sites (#1,201 thru 1,209)
Set gv_wafer_num to 5 for die tested in this .stdf

637980_5_ad53510PC_trm_doc_092000_170844.stdf

Site 3 Version 0 Yield 19/24

637980_5_ad53510PC_trm_doc_092000_162647.stdf

Site 9 Version 4 MET-3 T-COILS Yield 17/24

Cpk Analysis Utility Version 2.40

Limit File: 637980_5_ad53510PC_trm_doc_092000_184151.stdf

File Analyzed: 637980_5_ad53510PC_trm_doc_092000_184151.stdf

Tester: CTS 5010 Station: 1 Node: doc Exec: 5010_1.9.3e Sdf Ver: 4 Cpu: 1

Prober: Operator: eng

Job: /prod/dfst.load Lot: 637980 Sublot: Tested: 24 Pass: 17 Yield: 70.83%

File Analyzed: 637980_5_ad53510PC_trm_doc_092000_182850.stdf

Tester: CTS 5010 Station: 1 Node: doc Exec: 5010_1.9.3e Sdf Ver: 4 Cpu: 1

Prober: Operator: eng

Job: Lot: 637980 Sublot: Tested: 24 Pass: 19 Yield: 79.17%

File Analyzed: 637980_5_ad53510PC_trm_doc_092000_181452.stdf

Tester: CTS 5010 Station: 1 Node: doc Exec: 5010_1.9.3e Sdf Ver: 4 Cpu: 1

Prober: Operator: eng

Job: Lot: 637980 Sublot: Tested: 3 Pass: 2 Yield: 66.67%

File Analyzed: 637980_5_ad53510PC_trm_doc_092000_170844.stdf

Tester: CTS 5010 Station: 1 Node: doc Exec: 5010_1.9.3e Sdf Ver: 4 Cpu: 1

Prober: Operator: eng

Job: /prod/dfst.load Lot: 637980 Sublot: Tested: 20 Pass: 15 Yield: 75.00%

File Analyzed: 637980_5_ad53510PC_trm_doc_092000_162647.stdf

Tester: CTS 5010 Station: 1 Node: doc Exec: 5010_1.9.3e Sdf Ver: 4 Cpu: 1

Prober: Operator: eng

Job: /prod/dfst.load Lot: 637980 Sublot: Tested: 24 Pass: 8 Yield: 33.33%

Combined Lots Tested: 95 Pass: 61 Yield: 64.21%

Numb	Test Name	Valid Tests	Qty	Stat	Test Limits	Statistic Data Range	Mean	Units	Pos	Limit	Units	Std Dev	Limit Spn	CPK	% Exe	Fail	Notes
1	REV DATE	95	95	95	0	999999.00	92000.000	92000.000	-81.60	0	0.00	0	0.00	Inf			
2	perf_id	95	95	95	0	9.0000000	0	0	-100.00	0	0.00	0	0.00	NaN			
3	board_id	95	95	95	0	9.0000000	0	0	-100.00	0	0.00	0	0.00	NaN			
4	ring_id	95	95	95	0	9.0000000	1.0000000	1.0000000	-77.78	0	0.00	0	0.00	Inf			
5	contact_id	95	95	95	0	9.0000000	1.0000000	1.0000000	-77.78	0	0.00	0	0.00	Inf			
20	al_die_align PASSE	95	95	95	-0.9000000	0.9000000	0	0	0.00	0	0.00	0	0.00	Inf			
10	Opens Continuity	95	95	95	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	2.11		
11	Short Continuity	95	95	95	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	6.32		
12	PadNum Continuity	95	95	95	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	6.32		
13	PinNum Continuity	95	95	95	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail	Pass Fail			
14	Edgesense R	95	94	94	500.00000	1000.0000	767.78931	828.19568	11.92	779.81049	9.8169584	1.96	1.96	7.48	1.05		
15	NCY7_R	95	94	94	0	2500.0000	148.00000	293.00000	-80.37	55.395977	2.22	2.22	2.22	1.48	1.05		
16	DieVersion	95	95	95	0	4.0000000	-1.000000	4.0000000	-50.00	1.7564471	43.91	43.91	43.91	0.19	1.05		
17	TO PreTrim	95	93	93	0	100.00000	29.608751	74.863960	8.08	10.580537	10.58	10.58	10.58	1.45	2.11		
22	Laser Power uJ	95	95	95	0.2000000	1.5000000	0.3500000	0.5000000	-67.13	0.0367873	2.83	2.83	2.83	1.94			
24	Tsnr PreTrim	95	94	94	3000.0000	8000.0000	5073.1646	5411.3257	-13.20	62.738003	1.25	1.25	1.25	11.53	1.05		
25	Tsnr Trimmed	95	94	94	4500.0000	5500.0000	5075.5205	5411.3247	34.25	62.644276	6.26	6.26	6.26	1.75	1.05		
26	T2 Trim7sns	95	93	93	65.000000	75.000000	68.759850	72.039436	11.15	0.5401545	5.40	5.40	5.40	2.74	2.11		
100	lvcc_sns2	95	94	94	6.0000000	10.000000	8.062408	8.0344076	0.76	0.0037462	0.09	0.09	0.09	176.60	1.05		
101	lvcc_sns2	95	92	92	-8.000000	-4.000000	-6.008752	-5.995336	-0.25	0.0027130	0.07	0.07	0.07	245.12	1.05		
102	lvcc_vdd	95	95	95	1.3000000	2.3000000	1.7989486	1.7992352	-0.15	0.001363	0.01	0.01	0.01	1221.36	1.05		
103	lvcc_err	95	94	94	-0.3000000	0.2000000	-0.0087595	0.0194073	20.10	0.0037462	0.75	0.75	0.75	17.77	1.05		
104	lvcc_err	95	92	92	-0.2000000	0.3000000	0.0112476	0.0246644	-13.98	0.0027130	0.54	0.54	0.54	26.42	1.05		
105	lvdd_err	95	95	95	-0.0540000	0.0540000	-0.0010513	-0.002667	-1.42	0.001363	0.13	0.13	0.13	130.24	1.05		
106	lvdd_err	95	91	91	0.4000000	1.5000001	0.5746000	0.7639000	-49.86	0.0244700	0.22	0.22	0.22	3.76	1.05		
107	lvdd_err	95	91	91	-1.5000000	-0.4000000	-1.112900	-0.9970000	-18.71	0.0197035	1.79	1.79	1.79	7.56	1.05		
108	lvdd_err	95	91	91	-0.0500000	0.0500000	0.0155030	0.0165231	32.17	0.002514	0.25	0.25	0.25	44.98	2.11		
109	lvdd_err	95	89	89	6.0000000	15.000000	10.954113	12.540612	28.10	0.2654412	2.95	2.95	2.95	4.06	2.11		
110	lvcc_sns1	95	92	92	6.0000000	10.000000	8.0006723	8.0485315	1.18	0.0094014	0.24	0.24	0.24	70.07	2.11		
111	lvcc_plane	95	93	93	6.0000000	10.000000	8.0632801	8.1034517	3.89	0.0079888	0.20	0.20	0.20	80.21			

Numb	Test Name	Valid Tests	Stat Qty	Test Limits Min	Test Limits Max	Statistic Data Range Min	Statistic Data Range Max	Mean Units	Pos Limit	Units	Std Dev	Limit Spm	CPK	% Exe Fail	Notes
112	{vee_sns1	95	92	-8.000000	-4.000000	-6.117024	-5.964578	-6.052185	-2.61	0.0210411	0.53	0.53	30.86	2.11	
113	{vee_plane	95	93	-8.000000	-4.000000	-6.220200	-6.058495	-6.132965	-6.65	0.0173310	0.43	0.43	35.91		
114	{gnd_sense	95	92	-0.500000	0.500000	-0.0405250	-0.0112598	-0.0278871	-5.58	0.0039322	0.39	0.39	40.02	1.05	
115	{gnd_sense	95	92	-0.500000	0.500000	-0.0402112	-0.0112598	-0.0280142	-5.60	0.0038714	0.39	0.39	40.64	1.05	
116	{edge_sense	95	91	-0.500000	0.500000	-0.0381266	-0.0225936	-0.0273299	-5.47	0.0027303	0.27	0.27	57.71		
117	{lncy7	95	93	-0.500000	0.500000	-0.0203535	-0.0080356	-0.0106679	-2.01	0.0018788	0.19	0.19	86.92	1.05	
118	{lring Gnd	95	95	-0.500000	0.500000	0.0027060	0.0033336	0.0029818	0.60	0.0001178	0.01	0.01	1406.97		
130	IDLE_P1	95	92	0.0004500	0.0015000	0.0007962	0.0008499	0.0008314	27.36	1.111e-05	1.06	1.06	11.45	3.16	
131	IDLE_P2	95	94	0.0004500	0.0015000	0.0007779	0.0008570	0.0008343	-26.79	1.327e-05	1.26	1.26	9.65	1.05	
132	IDLE_N1	95	93	-0.0015000	-0.0004500	-0.0007779	-0.0008570	-0.0008343	22.77	1.637e-05	1.56	1.56	8.25	3.16	
133	IDLE_N2	95	90	-0.0015000	-0.0004500	-0.0008969	-0.0008031	-0.0008555	23.33	1.734e-05	1.65	1.65	7.74		
134	T_SLRD1	95	91	0.0004000	0.0030000	0.0017936	0.0019061	0.0018729	13.30	2.134e-05	0.82	0.82	17.61	2.11	
135	T_SLRD2	95	91	0.0004000	0.0030000	0.0019399	0.0022120	0.0020325	25.58	3.321e-05	1.28	1.28	9.71	1.05	
136	T_SLFD1	95	92	-0.0030000	-0.0040000	-0.0019231	-0.0017141	-0.0018377	-10.59	3.145e-05	1.21	1.21	12.32	1.05	
137	T_SLFD2	95	91	-0.0030000	-0.0040000	-0.0019019	-0.0017189	-0.0018322	-10.17	2.959e-05	1.14	1.14	13.16	1.05	
138	IMON_DC	95	94	0.0010000	0.0020000	0.0013363	0.0014984	0.0014203	-15.93	2.668e-05	2.67	2.67	5.25	1.05	
139	IMON_AC	95	92	0.0010000	0.0020000	0.0013491	0.0014502	0.0014119	-17.61	1.762e-05	1.76	1.76	7.79	3.16	
140	T_DIG_DC_MON	95	93	-0.0020000	-0.0010000	-0.0014400	-0.0013020	-0.0014020	19.60	2.22e-05	2.22	2.22	6.04		
160	AB1_VL_FUNCN1	95	88	-1.500000	0.800000	-1.188696	-1.148132	-1.174390	-6.97	0.0070413	1.01	1.01	15.41	6.32	
161	AB1_VL_OFFS	95	88	-0.400000	0.200000	-0.2065445	-0.1650396	-0.1911870	-30.40	0.0073228	1.22	1.22	9.51	4.21	
162	AB1_VL_FUNCN3	95	87	1.200000	0.400000	3.0432317	3.0873256	3.0616252	-34.59	0.0085048	1.06	1.06	10.25	6.32	
163	AB1_VH_FUNCN1	95	87	2.800000	3.599999	3.0432317	3.0873256	3.0616252	53.87	0.0154949	1.94	1.94	3.97		
164	AB1_VH_OFFS	95	86	3.700000	4.599999	4.1005464	4.2542481	4.2278857	66.17	0.0180570	3.01	3.01	1.87	5.26	
165	AB1_VH_FUNCN4	95	90	-0.200000	0.400000	-0.6161010	-0.5578843	-0.5845199	17.31	0.0210051	0.85	0.85	18.31	8.42	
170	AB2_VL_FUNCN1	95	83	-1.500000	0.800000	-1.186420	-1.156214	-1.172965	-6.56	0.0059547	1.07	1.07	10.95	10.53	
171	AB2_VL_OFFS	95	83	-0.400000	0.200000	-0.2035630	-0.1702179	-0.1899934	-30.00	0.0063909	1.07	1.07	10.95	10.53	
172	AB2_VL_FUNCN3	95	83	-0.400000	0.200000	-0.2035630	-0.1702179	-0.1899934	-30.00	0.0063909	1.07	1.07	10.95	10.53	
173	AB2_VH_FUNCN1	95	87	2.800000	3.599999	3.0506852	3.0908563	3.0637746	62.81	0.0241635	3.02	3.02	2.05	7.37	
174	AB2_VH_OFFS	95	87	-1.200000	-0.400000	-0.6571351	-0.5148888	-0.5487434	77.93	0.0253665	4.23	4.23	0.87	8.42	
175	AB2_VH_FUNCN4	95	84	3.700000	4.599999	4.1661382	4.3353748	4.2680831	26.24	0.0206646	2.30	2.30	5.35	7.37	
180	ROUT_1 VL+50	95	92	35.000000	55.000000	34.722862	50.442924	45.897110	8.97	2.1174841	10.59	10.59	1.43	4.21	
181	ROUT_1 VH-50	95	92	35.000000	55.000000	40.058083	50.824238	45.845787	8.46	1.8597041	9.30	9.30	1.64	3.16	
182	ROUT_2 VL+50	95	94	35.000000	55.000000	39.675198	47.632523	44.741272	-2.59	1.1311038	5.66	5.66	2.87	1.05	
183	ROUT_2 VH-50	95	92	35.000000	55.000000	47.76886	45.538006	45.538006	5.38	0.8413368	4.21	4.21	3.75	3.16	
2000	Part ID	95	95	0	999.00000	1.0000000	924.00000	370.69473	-25.79	319.51089	31.98	31.98	0.39		
2130	IDLE_P1	95	91	0.0004500	0.0005500	0.0005000	0.0005099	0.0005074	14.84	1.96e-06	1.96	1.96	7.24	3.16	
2131	IDLE_P2	95	94	0.0004500	0.0005500	0.0004755	0.0004999	0.0004897	-20.61	6.095e-06	6.10	6.10	2.17	1.05	
2132	IDLE_N1	95	94	-0.0005500	-0.0004500	-0.0004999	-0.0004661	-0.0004907	18.55	7.516e-06	7.52	7.52	1.81	1.05	
2133	IDLE_N2	95	92	-0.0005500	-0.0004500	-0.0004997	-0.0004731	-0.0004896	20.71	6.986e-06	6.99	6.99	1.89	3.16	
2134	T_SLRD1	95	88	0.0004000	0.0007000	0.0005090	0.0005576	0.0005233	-17.78	8.005e-06	2.67	2.67	5.14	3.16	
2135	T_SLRD2	95	92	0.0004000	0.0007000	0.0003106	0.0007031	0.0005482	-1.20	5.872e-05	19.57	19.57	0.84	7.37	
2136	T_SLFD1	95	93	-0.0007000	-0.0004000	-0.0005249	-0.0004721	-0.0005129	24.72	1.085e-05	3.62	3.62	3.47	2.11	
2137	T_SLFD2	95	93	-0.0007000	-0.0004000	-0.0005300	-0.0004755	-0.0005088	27.47	1.284e-05	4.28	4.28	2.83	2.11	
2180	ROUT_1	95	89	48.000000	52.000000	49.892139	50.347202	49.962582	-1.87	0.0643487	2.53	2.53	10.15	5.26	
2181	ROUT_2	95	93	48.000000	52.000000	49.784916	50.276588	50.087082	4.35	0.1012987	1.61	1.61	6.29	2.11	
3100	{vcc_sns2	95	93	6.000000	10.000000	8.0068684	8.0216970	8.0143623	0.72	0.028898	0.07	0.07	229.04		
3101	{vcc_sns2	95	92	-8.000000	-4.000000	-6.008360	-5.995257	-6.004480	-0.22	0.0026217	0.07	0.07	253.72		
3102	{act_vdd	95	95	1.300000	2.300000	1.7993410	1.7998902	1.7995623	-0.09	0.0001115	0.01	0.01	1492.93	1.05	
3103	{vcc_err	95	93	-0.300000	0.300000	-0.0081320	0.006967	-0.006379	19.74	0.0028898	0.58	0.58	23.14	1.05	
3104	{vdd_err	95	92	-0.200000	0.200000	0.0116401	0.0247426	0.0155196	-13.79	0.0026217	0.52	0.52	27.40	1.05	
3105	{vdd_err	95	95	-0.0540000	0.0540000	-0.0006590	-0.0001098	-0.0004376	-0.81	0.0001115	0.10	0.10	160.07		
3106	{max_ice	95	89	0.400000	1.500000	0.5102000	0.6094000	0.5482809	-73.04	0.0158343	1.44	1.44	3.12	1.05	
3107	{max_ice	95	91	-1.500000	-0.400000	-0.9875000	-0.8653000	-0.9279022	32.20	0.002607	1.33	1.33	12.01	2.11	
3108	{max_ice	95	91	-0.0500000	0.0500000	0.0155030	0.0161020	0.0161020	4.02	0.0146468	0.26	0.26	43.35	2.11	
3109	{max_power	95	89	6.000000	15.000000	9.4697561	10.842550	9.9911985	-11.31	0.0029172	2.25	2.25	6.56	1.05	
3110	{vcc_sns1	95	92	6.000000	10.000000	8.0203648	8.0569267	8.0350609	1.75	0.0072249	0.18	0.18	90.66	2.11	
3111	{vcc_plane	95	93	6.000000	10.000000	8.0631237	8.0962334	8.0734377	3.67	0.0069605	0.17	0.17	92.26		
3112	{vcc_plane	95	92	-8.000000	-4.000000	-6.125419	-5.994706	-6.075070	-3.75	0.0172546	0.43	0.43	37.19	2.11	
3113	{vcc_plane	95	93	-8.000000	-4.000000	-6.194386	-6.056848	-6.127498	-6.37	0.0154205	0.39	0.39	40.48		
3114	{gnd_sense	95	92	-0.500000	0.500000	-0.0398973	-0.0103967	-0.0277038	-5.54	0.0039201	0.39	0.39	40.16	1.05	
3130	IDLE_P1	95	90	0.0004500	0.0005500	0.0005026	0.0005129	0.0005103	20.67	2.07e-06	2.02	2.02	6.55	3.16	

Numb	Test Name	Valid Tests	Stat Qty	Test Limits	Statistic	Data Range	Mean	Units	Std. Dev	Limit Spn	CPK	% Exe Fail	Notes
				Min	Max	Min	Max						
3131	IDLE_P2	95	94	0.0004500	0.0005500	0.0004780	0.0005295	0.0004929	-14.15	7.181e-06	7.18	1.99	1.05
3132	IDLE_N1	95	93	-0.0005500	-0.0004500	-0.0005018	-0.0004877	-0.0004923	15.32	7.752e-06	7.75	1.82	2.11
3133	IDLE_N2	95	91	-0.0005500	-0.0004500	-0.0005019	-0.0004749	-0.0004917	16.52	7.005e-06	7.00	1.99	4.21
3134	T_SLRD1	95	89	0.0004000	0.0007000	0.0005141	0.0005694	0.0005296	-13.59	9.201e-06	3.07	4.70	3.16
3135	T_SLRD2	95	92	0.0004000	0.0007000	0.0003091	0.0007040	0.0005481	-1.24	5.897e-05	19.66	0.84	7.37
3136	T_SLRD1	95	93	-0.0006000	-0.0004000	-0.0005253	-0.0004723	-0.0005130	-13.03	1.089e-05	5.45	2.66	2.11
3137	T_SLRD2	95	93	-0.0006000	-0.0004000	-0.0005277	-0.0004752	-0.0005081	-8.14	1.296e-05	6.48	2.36	2.11
3138	IMON_DC	95	94	0.0012000	0.0018000	0.0013361	0.0014981	0.0014204	-26.53	2.671e-05	4.45	2.75	1.05
3139	IMON_AC	95	92	0.0017500	0.0018000	0.0013489	0.0014508	0.0014123	-29.22	1.768e-05	2.95	4.00	3.16
3140	DIG_IMON	95	93	-0.0012500	-0.0012500	-0.0014400	-0.0013020	-0.0014021	39.14	2.233e-05	4.45	2.28	2.11
3151	T_SLRD1_I00	95	90	0.0001500	0.0005000	0.0003875	0.0004608	0.0004005	43.17	1.292e-05	3.69	2.57	4.21
3152	T_SLRD1_I00	95	93	-0.0006000	-0.0004000	-0.0005250	-0.0004722	-0.0005129	-12.89	1.085e-05	5.43	2.68	2.11
3153	T_SLRD2_I00	95	93	0.0001500	0.0005000	3.015e-08	0.0005150	0.0002897	-20.18	6.972e-05	19.92	0.67	7.37
3154	T_SLRD2_I00	95	93	-0.0006000	-0.0004000	-0.0005275	-0.0004751	-0.0005080	-8.00	1.279e-05	6.39	2.40	2.11
3155	T_SLRD1_I64	95	89	0.0005000	0.0009500	0.0006370	0.0007047	0.0006616	-28.18	1.104e-05	2.45	4.88	3.16
3156	T_SLRD1_I64	95	93	-0.0006000	-0.0004000	-0.0005252	-0.0004724	-0.0005130	-13.03	1.097e-05	5.48	2.64	2.11
3157	T_SLRD2_I64	95	93	0.0005000	0.0009500	0.0005150	0.0010172	0.0008097	37.66	7.347e-05	16.33	0.64	5.26
3158	T_SLRD2_I64	95	93	-0.0006000	-0.0004000	-0.0005276	-0.0004700	-0.0005083	-8.35	1.317e-05	6.59	2.32	2.11
3160	AB1_VL_FUNCN1	95	88	-1.300000	-0.700000	-1.015693	-0.9909786	-1.004729	-1.58	0.0047940	0.80	20.53	5.26
3161	AB1_VL_OFFS	95	89	-0.300000	0.200000	-0.0255393	-0.0023154	-0.0152612	13.90	0.0044245	0.88	16.22	5.26
3162	AB1_VL_FUNCN3	95	88	3.000000	3.599999	3.2495792	3.2735875	3.2591386	-13.62	0.0042936	0.72	20.12	6.32
3163	AB1_VH_FUNCN1	95	87	-1.200000	-0.600000	-0.7897310	-0.7573274	-0.7736550	42.12	0.0064150	1.07	9.02	5.26
3164	AB1_VH_OFFS	95	88	-0.200000	0.300000	0.1007798	0.1373418	0.1157272	26.29	0.0067261	1.35	9.13	5.26
3165	AB1_VH_FUNCN4	95	87	3.700000	4.300002	4.0644555	4.0912886	4.0760007	25.33	0.0065416	1.09	11.41	7.37
3170	AB2_VL_FUNCN1	95	88	-1.300000	-0.700000	-1.047331	-0.9819558	-1.009852	-3.28	0.0071838	1.20	13.46	5.26
3171	AB2_VL_OFFS	95	88	-0.300000	0.200000	-0.0566091	0.0070997	-0.0202638	11.89	0.0068148	1.36	10.77	6.32
3172	AB2_VL_FUNCN3	95	88	3.000000	3.599999	3.2188232	3.2792366	3.2540638	-15.31	0.0063338	1.06	13.37	6.32
3173	AB2_VH_FUNCN1	95	87	-1.200000	-0.600000	-0.838250	-0.6926771	-0.7403099	53.23	0.0216058	3.60	2.16	8.42
3174	AB2_VH_OFFS	95	87	-0.200000	0.300000	0.0560582	0.1956369	0.1481818	39.27	0.0217866	4.36	2.32	7.37
3175	AB2_VH_FUNCN4	95	88	3.700000	4.300002	4.0207534	4.1903820	4.1083293	36.11	0.0219003	3.65	2.92	6.32

NOTES:

1. There are no test limits for this Parameter in the Limit File. The Cpk is calculated using the limits found in the File Analyzed.
2. Asymmetrical Guardband limits. The Cpk refers to the high limit only.
3. Asymmetrical Guardband limits. The Cpk refers to the low limit only.
4. No test limits. The Cpk, Mean position and Std. Dev. \$Limit Spn could not be calculated for this test.
6. Alarms detected on 1 or more parts. These parts are not included in the 'Valid Tests' quantity or the statistics.

S# This data represents the statistics for one specific test site.

Parameter	637980	637980	637980.5	637980	637980	COMBINED LOTS
Qty of Parts Tested	24	24	3	20	24	95
Qty of Parts PASS	17	19	2	15	8	61
Yield	70.83%	79.17%	66.67%	75.00%	33.33%	64.21%
Total Devices Binned	24	24	3	20	24	95
Bin 1	17	19	2	15	8	61
Yield	70.83%	79.17%	66.67%	75.00%	33.33%	64.21%
Bin 11	0	0	0	0	1	1
Yield	0.00%	0.00%	0.00%	0.00%	4.17%	1.05%
Bin 97	7	5	1	5	15	33
Yield	29.17%	20.83%	33.33%	25.00%	62.50%	34.74%

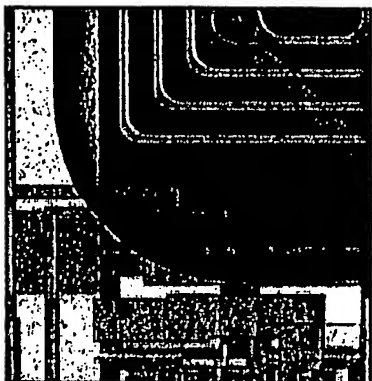


DATE: October 12th, 2000
TO: Rick Morrison
FROM: Justin Borski

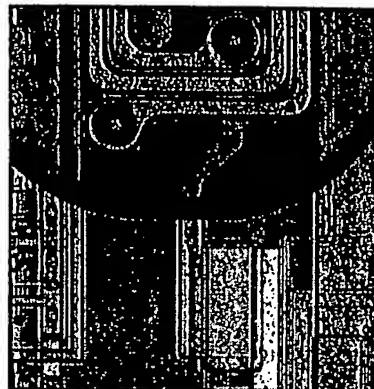
SUBJ: First T-COIL PC-10 Wafer Delivered!

Rick, below please find information pertaining to each wafer delivered in this shipment. There are VMI wafer defect maps associated with each T-COIL product wafer included in this shipment. Prior to post-wafer assembly, these wafers should be inspected to ensure selection of functional die based on the VMI maps. Engineering data and items of interest include:

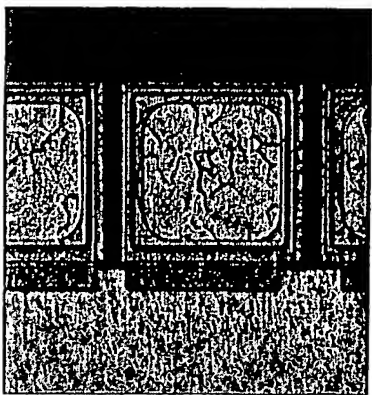
- Wafers 02B5 and 2111 (non-int.) have AMS-deposited encapsulation of 0.5 μ m Al₂O₃. The aluminum oxide has been reactively etched away from on top of all but two thin-film trim resistors. The two trim resistors effected are shown in picture (1).
- Wafers 06D6 and 2112 (non-int.) DO NOT have AMS encapsulation.
- Shown below are some relevant pictures of design and/or device issues to be aware of during packaging and test:



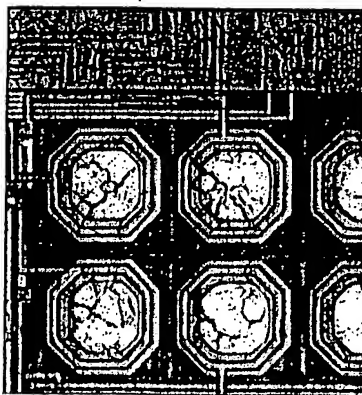
1.) Thin-film trim resistors covered by insulator



2.) Uncovered thin-film trim resistors, wafer 02B5



3.) Non-conductive ring area on aluminum bond pad, wafer 02B5



4.) Probe-points area reduction; wafer 06D6 conductive, wafer 02B5 non-conductive



- Key measurement data taken during AMS post-processing:

Ruthenium Barrier

Rs (ohms/sq)	Non-uniformity (%)
1.61	0.3

Insulator Thickness

Wafer ID	Thickness Mean (μm)	Thickness Range (μm)
2111	7.5	0.2
2112	7.7	0.1

Copper Coil Thickness

Wafer ID	Thickness Mean (μm)	Thickness Range (μm)
2111	5.6	0.5
2112	6.3	0.5
02B5	6.7	0.6
06D6	7.0	0.5

Aluminum Oxide Encapsulation

Thickness Mean (ang)	Non-uniformity (%)
4980	1.5

BOX 1, 4 T-COIL WAFERS

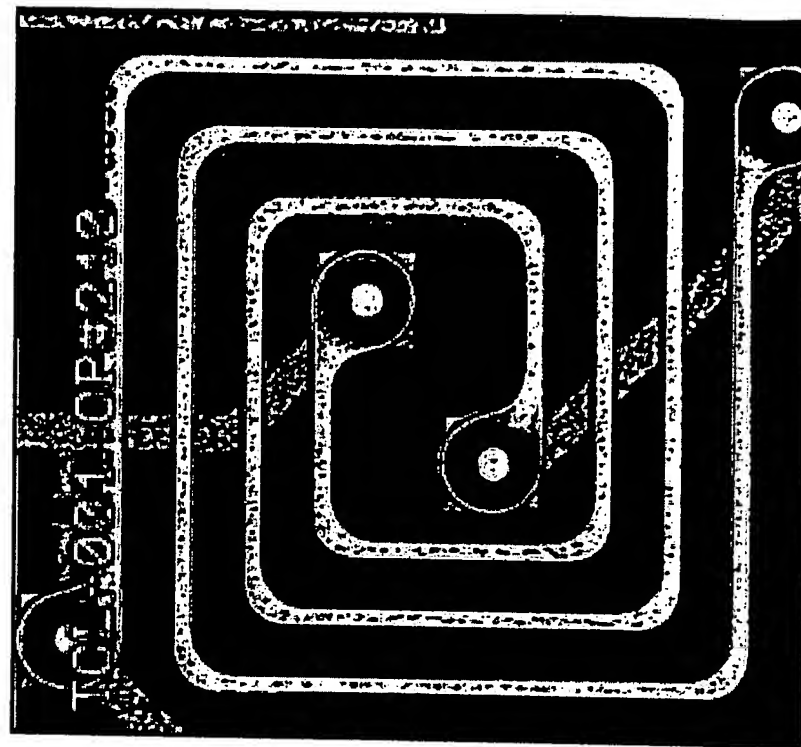
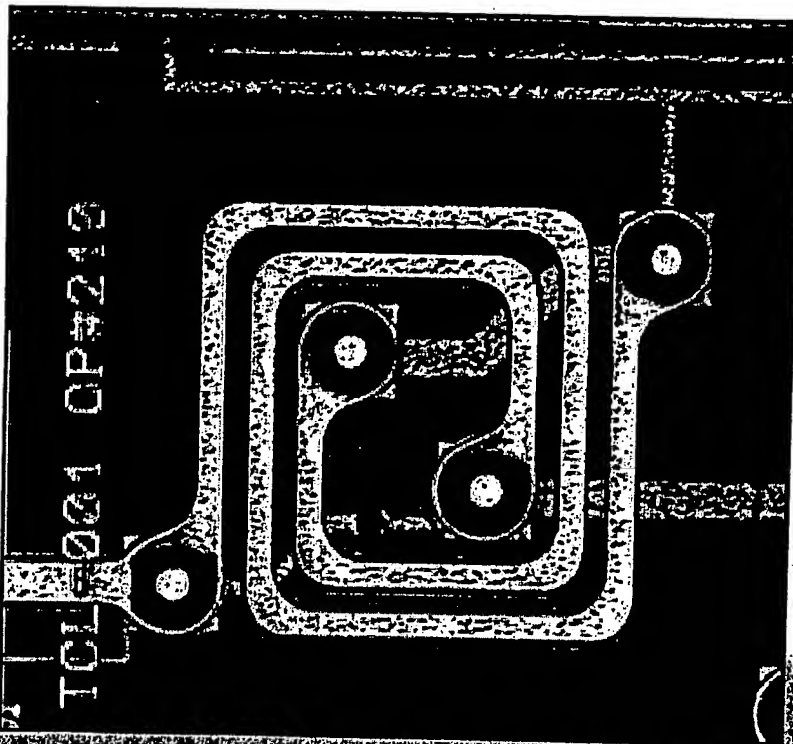
SLOT	WAFER ID	LOT - DESCRIPTION
25		
24		
23		
22		
21		
20		
19		
18		
17		
16		
15		
14		
13		
12		
11		
10	06D6	TCL-002
9		
8	2112	TCL-002
7		
6		
5		
4	02B5	TCL-002
3		
2	2111	TCL-002
1		

Regards,

Justin C. Borski
Advanced MicroSensors Inc.

Advanced MicroSensors Confidential

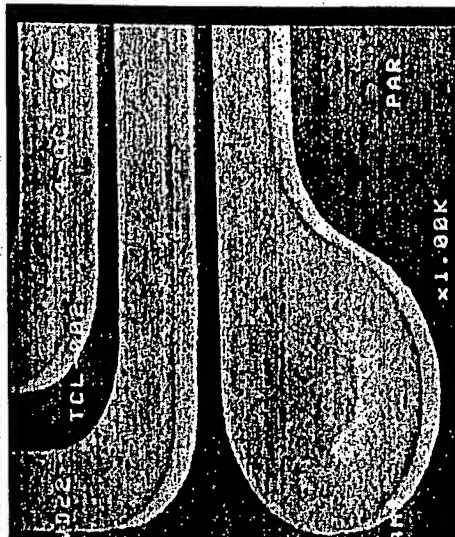
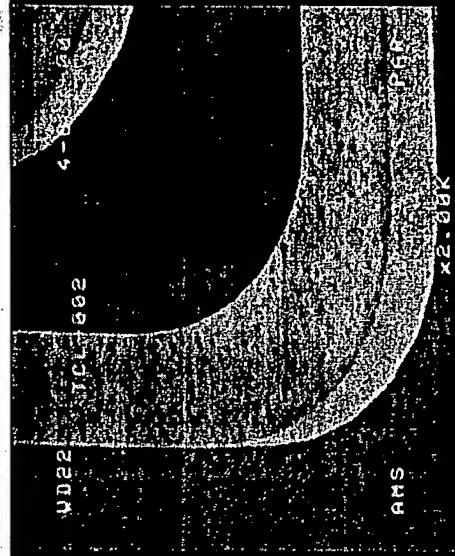
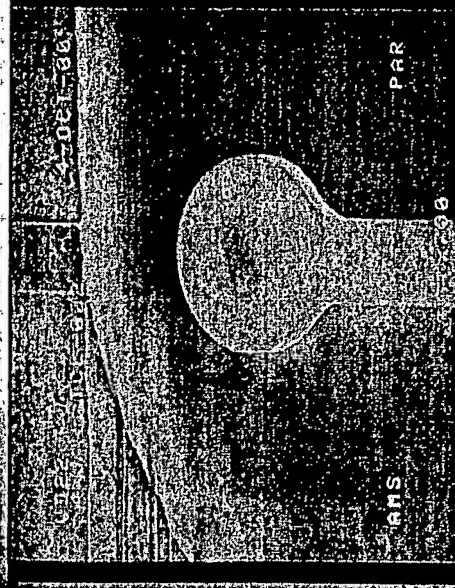
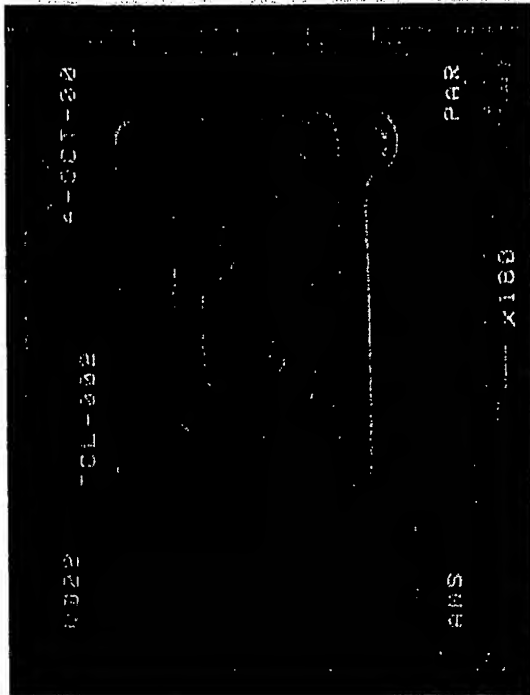
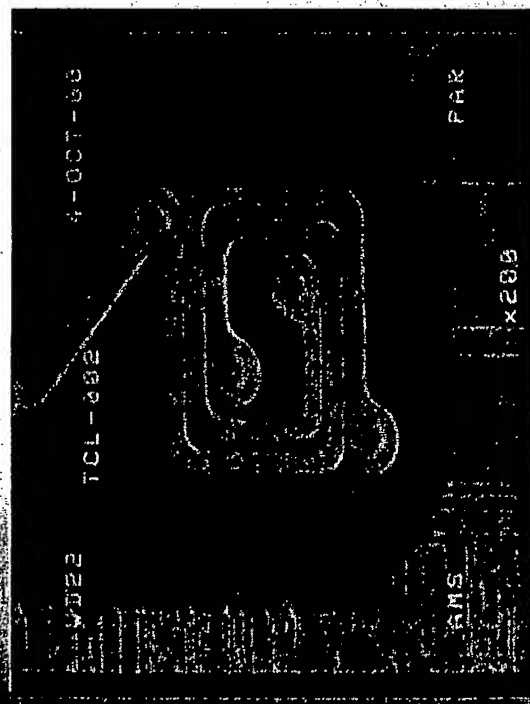
First On-Chip T-Coils (1)



ADI Proprietary
1



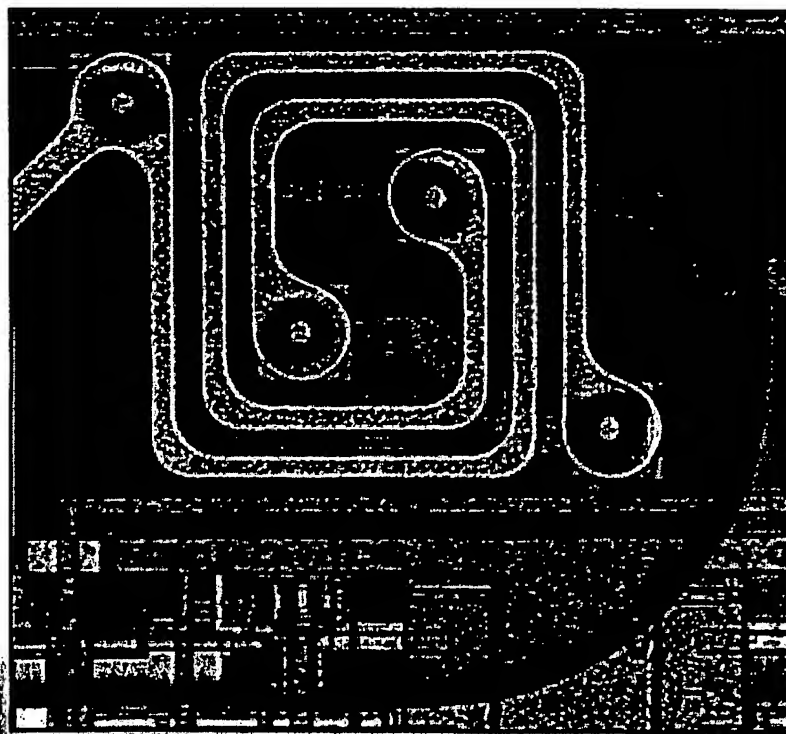
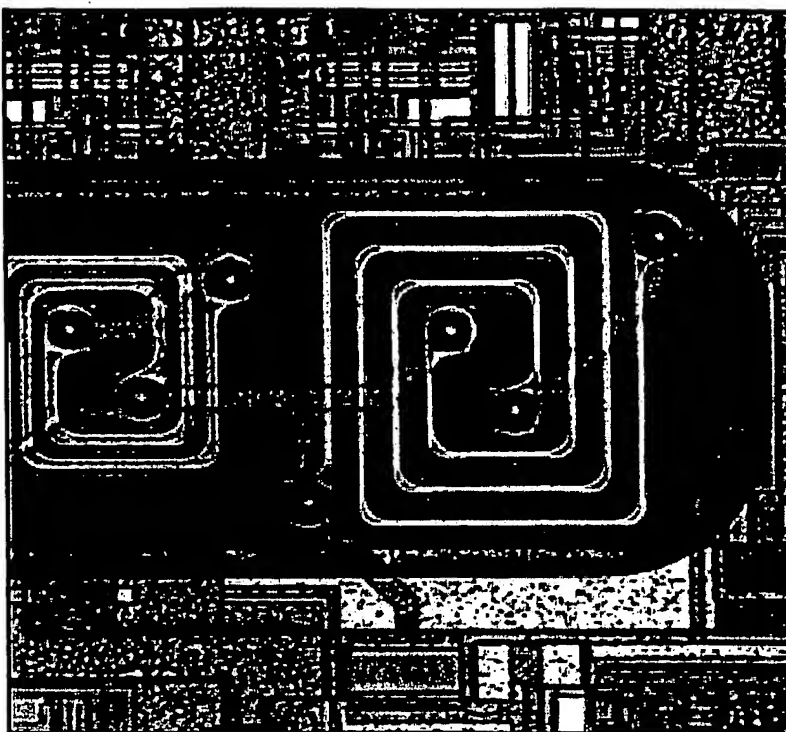
First On-Chip T-Coils (2)



ADI Proprietary
2



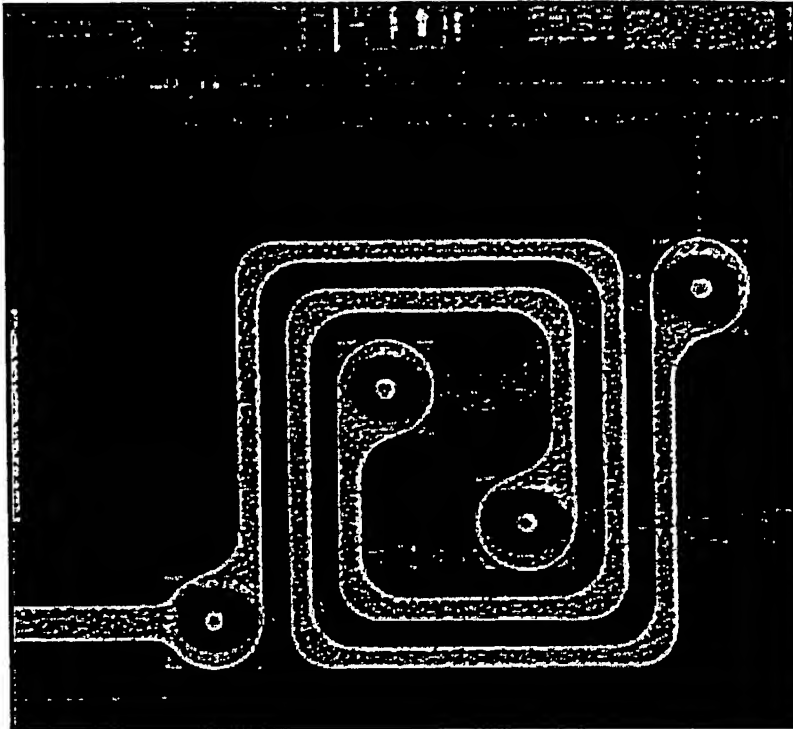
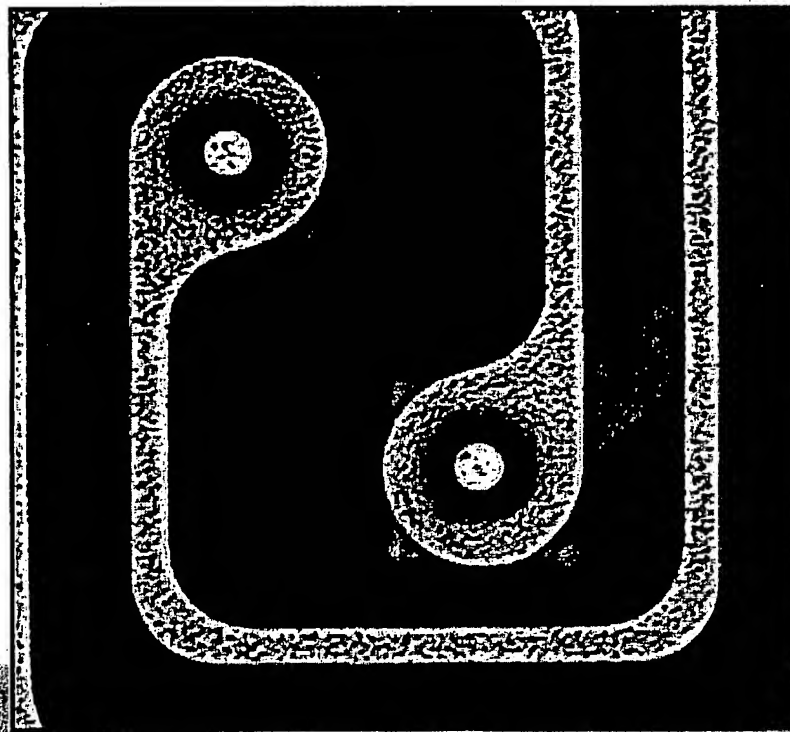
First On-Chip T-Coils (3)



ADI Proprietary
3



First On-Chip T-Coils (4)



ADI Proprietary
4



11801C DIGITAL SAMPLING OSCILLOSCOPE
date: 17-OCT-00 time: 10:02:59

Tek



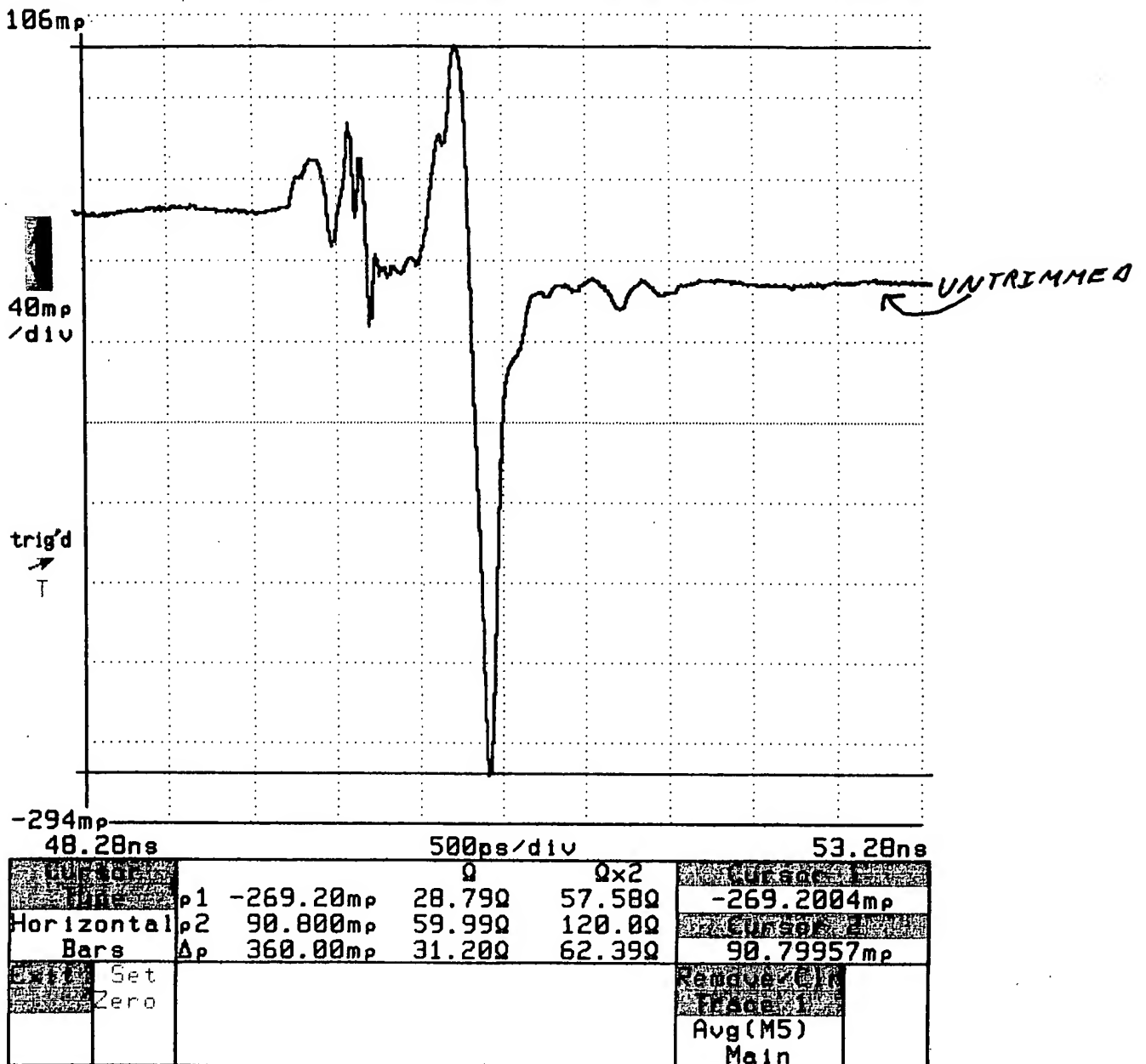
Cursor 1		Cursor 2	
Type		50.58000ns	
Vertical Bars		Cursor 2	
52.67000ns		Remove/Clr	
Set	t1 50.580ns	t1/2 25.290ns	Trace 1
Zero	t2 52.670ns	t2/2 26.335ns	Avg (M5)
	Δt 2.090ns	$\Delta t/2$ 1.045ns	Main
	$1/\Delta t$ 478.47MHz		

PIN 1
PROBES DOWN
POWER ON

OUT WITH TCOILS

11801C DIGITAL SAMPLING OSCILLOSCOPE
date: 18-OCT-00 time: 14:46:24

Tek



PIN 1
PROBES DOWN
POWER ON
BUT WITHOUT T COILS

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